Electrothermal Simulation and Characterisation of Series Connected Power Devices and Converter Applications

By

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Declaration

This thesis is submitted to the University of Warwick in support of the application for the degree of Doctor of Philosophy. The work presented in this thesis was carried out in the School of Engineering, University of Warwick, during the period May 2015 to August 2018 under the supervision of Dr Olayiwola Alatise. It has not been submitted in part, or in whole, for a degree or other qualification at any other University. Parts of this thesis are published by the author in peer-reviewed research papers listed. Apart from commonly understood and accepted ideas, or where reference is made to the work of others, the work described in this thesis is carried out by the author.

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To my family.

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Publication List

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2. **Z. Davletzhanova**, O. Alatise, J. O. Gonzalez, S. Konaklieva and R. Bonyadi, "Electrothermal Stresses in SiC MOSFET and Si IGBT 3L-NPC Converters for Motor Drive Applications," *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Nuremberg, Germany, 2017, pp. 1-8.

3. **Z. Davletzhanova**, O. Alatise, R. Bonyadi, J. O. Gonzalez and T. Dai, "Characterization of Voltage Divergence in Series Connected SiC Trench MOSFETs and Si IGBTs," *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Nuremberg, Germany, 2018, pp. 1-7.

4. Bonyadi, R; Alatise, O; Hu, J; **Davletzhanova, Z**; Bonyadi, Y; Ortiz-Gonzalez, J; Ran, L; Mawby, P.A, "Compact electrothermal models for unbalanced parallel conducting Si-IGBTs," *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016, pp. 253-260.

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8. **Davletzhanova, Z**; Alatise, O; Gonzalez, J. A. O; Bonyadi, R; Dai, T; Chan, C W; Mawby, P, "Safe-Operating-Area of Snubberless Series Connected Silicon and SiC power devices", 2018 IEEE 10th Annual Energy Conversion Congress and Exposition (ECCE 2018), Portland, 2018.

Abstract

Power electronics is undergoing significant changes both at the device and at the converter level. Wide bandgap power devices like SiC MOSFETs are increasingly implemented in automotive, grid and industrial drive applications with voltage ratings as high as 1.7kV now commercially available although much higher voltages have been demonstrated as research prototypes. In high power applications where high DC bus voltages are used, as is the case in voltage source converters for industrial drives, marine propulsion and grid connected energy conversion systems, it may be necessary to series connect power devices for OFF-state voltage sharing. In high power applications, before the advent of multi-level converters, series connection of IGBT power modules was commonplace especially for HVDC-voltage source converter applications. However, with the advent of the modular multi-level converter, where the AC voltage waveform is synthesized by discrete voltage steps, the need for series connected is obviated. Most HVDC-VSC applications are now implemented by modular-multi-level converters.

However, in some applications like VSCs for distribution network power conversion, there can be a combination between series connection of power devices and multi-level converter. Traditionally, voltage balancing in series connected power devices was achieved using snubber capacitors for dynamic voltage sharing and resistors for static voltage sharing. However, the use of snubber capacitors reduces the switching speed of the converter thereby defeating the purpose of using SiC power devices especially in power converters with high switching frequencies. To avoid this, active gate driving techniques that avoid the use of snubber capacitors during switching are under intensive research focus. This involves intelligent gate drivers capable of dynamically adjusting the gate pulse during switching. To use these gate drivers, it is

necessary to explore the boundaries of static and dynamic voltage imbalance in series connected power devices. For example, it is necessary to understand how differences in device junction temperature and gate driver switching rates affects voltage divergence between series connected devices and how this differs between silicon IGBTs and SiC MOSFETs. This is similarly the case between series connected silicon PiN diodes and SiC Schottky diodes. Since silicon IGBTs and PiN diodes respectively exhibit tails currents and reverse recovery during turn-OFF, the dynamics of voltage divergence between series devices will differ from unipolar SiC power devices. Furthermore, the leakage current mechanisms determine the OFF-state voltage balancing dynamics and since Si IGBTs have different leakage current mechanisms from SiC devices, OFF-state voltage balancing in series connected devices will be different between the technologies.

The contribution of this thesis is using finite element and compact device models backed by experimental measurements to investigate static and dynamic voltage imbalance in series connected power devices. Starting from the fundamental physics behind device operation, this thesis explores how the leakage currents and tail currents affects voltage divergence in series silicon bipolar devices compared to SiC power devices. This analysis is compared with how the switching dynamics peculiar to fast switching SiC devices affects voltage balancing in series connected SiC devices. Simulations and measurements show that series connected SiC power devices are less prone of excessive voltage divergence due to the absence of tail currents compared to series connected silicon bipolar devices where voltage divergence due to tail currents is evident. Reduced leakage currents due to the wide bandgap in SiC also ensures that it is less prone to voltage divergence (compared to silicon bipolar devices) under static OFF-state conditions. This means the snubber resistances can be increased thereby reducing the OFF-state power dissipation in series connected SiC devices. In the

analysis of voltage sharing of series connected devices during the static ON-state and OFF-state it was shown that the zero-temperature coefficient of the power devices determines the voltage sharing and loss distribution in the ON-state while the leakage current and switching synchronization is critical in the OFF-state. Simulations and measurements in this thesis show that the higher ZTC points in silicon bipolar devices compared to SiC unipolar devices means that ON-state voltage divergence depends on the load current. The dominant failure mode for series connected power devices is failure under dynamic avalanche which occurs in cases of extreme uncontrolled voltage divergence. In the investigations of the switching transient behaviour of series connected IGBT and SiC MOSFETs during turn-OFF, it was shown that the voltage imbalance for Si IGBT is highly dependent on the carrier concentration in the drift region during switching while for SiC MOSFET it depends on the switching time constant of the gate voltage and the rate that the MOS-channel cuts the current. The thesis also explores the limits of power device performance under dynamic avalanche conditions for both series silicon bipolar and SiC unipolar devices. In the analysis of SOA of series connected devices it was discussed that the SOA is reduced by increased switching rates and DC link voltages. Finally, the thesis explores the 3L-NPC converter and how the power factor of the load on the AC side of the converter alters the power dissipation sharing between the devices. The results show that loss distribution between the devices in the converter is not just affected by the load power factor but also by the switching frequency.

List of Abbreviations

BJT	Bipolar Junction Transistor
CSR	Charge Storage Region
CTE	Coefficient of Thermal Expansion
DUT	Devices under test
ECCE	Energy Conversion Congress and Exposition
EV	Electric Vehicle
FACTS	Flexible Alternating Current Transmission System
FE	Finite Element
FEM	Finite Element Models
FMEA	Failure Mode and Effect Analysis
GaN	Gallium Nitride
GTO	Gate Turn-Off
HEV	Hybrid Electric Vehicle
HV	High Voltage
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
JFET	Junction Field Effect Transistors
KVL	Kirchhoff's current and voltage laws
LED	Light Emitting Diodes
LCC	Line-Commutated Converters
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistors
MMC	Modular Multilevel Converter
NPT	Non-Punch Through
NPC	Neutral Point Clamped
PHEV	Plug-in Hybrid Electric Vehicle
PMSM	Permanent magnet synchronous machine
PT	Punch Through

SiC	Silicon Carbide
SOA	Safe Operating Area
SPWM	Sinusoidal Pulse Width Modulation
SVM	Space Vector Modulation
VSC	Voltage source converters
VSI	Voltage source inverter

List of Symbols

A	Active die area (cm^2)
B_{VD}	Breakdown voltage of the device (V)
C_B	Drain-base capacitance of BJT (F)
C_{GD}	Gate-drain capacitance (F)
C_{ox}	Oxide capacitance per unit area (Fcm^{-2})
C_p	Specific heat ($W.kg^{-1}.K^{-1}$)
C_{th}	Thermal capacitance (J/K)
D_a	Ambipolar diffusivity (cm^2s^{-1})
D_n	Electron diffusivity (cm^2s^{-1})
D_p	Hole diffusivity (cm^2s^{-1})
E	Electric field (Vcm^{-1})
G_p	Hole generation rate ($cm^{-3}s^{-1}$)
g_m	Transconductance (S)
I_{AK}	Anode-cathode current (A)
I_{CE}	Collector-emitter current (A)
I_{DS}	Drain-source current (A)
I_d, I_q	Current components
I_g	Gate terminal current (A)
I_{GD}	Gate-drain current (A)
I_L	Leakage current (A)

I_{mos} MOS channel current (A)

I_n Electron current (A)

I_p Hole current (A)

J Current density due to electrons and holes ($cm^2V^{-1}s^{-1}$)

J_C Collector current density (Acm^{-2})

J_{CE} Collector-emitter current density (Acm^{-2})

J_F Forward current density (Acm^{-2})

J_L Leakage current density (Acm^{-2})

J_n Electron current density ($A.cm^{-2}$)

J_p Hole current density ($A.cm^{-2}$)

J_S Saturation current density (Acm^{-2})

J_{SC} Space-charge current density (Acm^{-2})

k Boltzmann constant ($\cong 1.381\times10^{-23}\,JK^{-1}$)

K_p MOS transconductance (AV^{-2})

K_{th} Thermal conductivity ($Wm^{-1}K^{-1}$)

L Length of inversion layer (cm)

L_a Ambipolar diffusion Length (cm)

l Length in the direction of charge flow (cm)

n Electron concentration (cm^{-3})

N_A Acceptor (P-type) doping concentration (cm^{-3})

N_B Drift region doping N-type concentration (cm^{-3})

N_D Doping concentration of N-type drift region (cm^{-3})

N_H Buffer layer doping (cm^{-3})

n_i Intrinsic carrier concentration (cm^{-3})

p Free hole concentration (cm^{-3})

q Unit electron charge ($\approx 1.6\times10^{-19}$C)

$Q_{channel}$ Charge in the inversion layer (C)

Q_f Fixed oxide charge (C)

$R_{1,2}$ Gate resistance (Ω)

R_{CH} The resistance of the channel (Ω)

R_{DS} Total on-state resistance (Ω)

R_{drift} Drift resistance (Ω)

R_G Series resistance (Ω)

R_L Leakage resistance (Ω)

R_S Parasitic series resistance (Ω)

R_{th} Thermal resistance (K/W)

T Temperature (K)

T_0 Reference temperature (≈300K)

T_{em} Mutual torque (N· m)

T_{ec} Cogging torque (N· m)

t_{ox} Oxide thickness (nm)

V Volume (m^3)

V_B Drift region voltage drop (V)

V_{CE} OFF-state voltage (V)

V_{CH} ON-state voltage of MOS channel (V)

V_d Depletion voltage (V)

v_d Drift velocity (cms^{-1})

V_{DS} Drain-source voltage (V)

V_{GS} Gate-source voltage (V)

V_{GP} Gate-plateau voltage (V)

V_{IGBT} ON-state voltage of IGBT (V)

V_{PIN} Forward voltage of PiN diode (V)

V_T Thermal voltage (V)

V_{th} Threshold voltage (V)

W Width of inversion layer (cm)

W_D Depletion width (cm)

W_d Width of drift layer (cm)

W_B Carrier storage region width (μm)

W_{cell} MOS cell width (μm)

W_{d1} Width of the depletion layer at anode end of the charge storage region (μm)

W_H IGBT buffer layer width (μm)

Z_{TH} Thermal impedance

Z_{th} Thermal impedance (K/W)

α_F Forward transfer ratio (typically ≈0.98)

α_{PNP} Open-base current gain of the PNP BJT

β MOS channel gain

μ Effective mobility ($cm^2V^{-1}s^{-1}$)

$\mu_{i,\max}$ Maximum mobility of electron/hole ($cm^2V^{-1}s^{-1}$)

μ_n Electron mobility ($cm^2V^{-1}s^{-1}$)

μ_p Free hole mobility ($cm^2V^{-1}s^{-1}$)

$\frac{\partial p}{\partial x}$	Gradient of free hole carrier density (cm^{-4})
ρ	Density ($kg.m^{-3}$)
τ	High-level carrier lifetime (s)
τ_{HL}	High-level carrier lifetime (s)
τ_n	Electron lifetime (s)
τ_p	Hole lifetime (s)
τ_{SC}	Space charge generation lifetime (s)
ε	Permittivity (Fcm^{-1})
ε_0	Permittivity of free space (Fcm^{-1})
ε_{ox}	Silicon oxide permittivity (Fcm^{-1})
ε_r	Relative permittivity
ε_s	Semiconductor permittivity (Fcm^{-1})
ε_{si}	Silicon permittivity (Fcm^{-1})
Φ_{bi}	Built-in potential (V)
ϕ_B	Bulk potential
ϕ_{BN}	Schottky barrier height
ϕ_{ms}	Work Function (eV)

Chapter

1 Introduction

1.1 Background

Process, conversion and control of flow of electric power in a circuit is enabled through application of solid-state technology and more specifically power electronic devices. Advancement of power electronic devices, resulted in more flexibility in the usage of different power forms and conversion of power from AC to DC and vice-versa or stepping up and down of DC voltage levels as well as AC to AC conversion. This contributes into the more efficient use of electricity at all power ranges and all different applications from conversion of power required in chargers of mobile phones and laptops, to conversion of power required in powertrain electrification for transportation to conversion of power in the grid connected converters used in applications such as HVDC and flexible AC transmission systems (FACTS) [1-4]. In these converters power semiconductor devices control the electrical power.

1.2 Power Semiconductor Devices

The power semiconductor devices are used to control power flow to the load using capacitors and inductors as energy storage elements. They act as switches operating in two states: on and off. Ideal power devices should not have any conduction or switching losses, however in reality there are no ideal devices. Conduction losses happen due to series resistances, off-state losses are due to leakage current and instantaneous switching losses are due to parasitic inductances, resistances and capacitances. Power semiconductor devices can be classified into two groups: two terminal devices such as PiN or Schottky diodes or three terminal devices such as thyristors and transistors.

Depending on the application, various types of power semiconductor devices are available. Diodes are non-controllable switches since on and off states are controlled by the power circuit [5]. Controllable switches like BJTs are turned on and off by control signals [6]. The creation of BJT in 1947 allowed to control the electricity by solid-state control. However, there was still limitation in the control of electrical power until 1950 when the thyristor was introduced. Thyristors are semi-controllable switches in the sense that they can be latched on by a control signal but can only be turned off by the power circuit [5,7]. However, based on the latest developments of the thyristor it became possible for the device to be turned off by gate signal like in gate turn-off thyristor (GTO) [8]. Therefore GTO can be used in more complex power conversion systems. However, the disadvantage of that technology is slow switching speed.

The MOSFET was developed with high voltage designs in the mid-1970s [9]. The advantages of MOSFETs are minimal drive requirements, voltage-controlled device and it has faster switching speed in comparison to the BJT or thyristor. However, the main disadvantage is poor power handling capabilities due to quite high on-state resistance compared to the thyristor. Later developments of WBG materials like SiC made MOSFETs available for medium voltage applications.

In the early 1980s, the concept of the IGBT was developed by combining the technologies of the MOSFET and BJT [10, 11]. The gate signal is applied to the MOSFET, providing the advantages of compact and low cost gate drive circuits allowed by high input impedance and voltage-controlled operation. The BJT is designed to carry most of the device current due to it low specific on-state resistance. Therefore the IGBT shares the advantages of both these devices. Currently, most converter technology is IGBT-based, since it has a valuable size and cost advantage compared to thyristor technology.

1.3 Research Objectives and Contribution

The focus of this thesis is on simulation and electrical characterisation of series connected power devices such as silicon PiN diodes, SiC Schottky diodes, silicon IGBTs

and SiC power MOSFETs. The electrothermal characteristics of these devices under clamped inductive switching conditions have been considered as series-connected devices. For some HV applications power devices are connected in series for high voltage blocking capability. They can also be connected in parallel to provide higher current, however it is out of scope of this thesis. The intrinsic problem with series connected devices is the voltage sharing between the devices which leads to unbalance electro-thermal stress on the devices. The unbalance voltage sharing can be a consequence of variation in the internal structure of the device and the manufacturing tolerances of the dies which is inevitable. The variations of the physical parameters of the devices which can lead to unbalanced voltage sharing are slight differences in the leakage current, carrier lifetime in the drift region, doping of the drift region, mobility of the carriers, threshold voltage and presence of defects on the crystal lattice (more applicable to SiC crystalline structure). In addition, differences in the circuit layout and different spread of electrical circuit parameters as well as non-uniform gate driver circuit leads to this unbalance voltage sharing. These are highly important and need to be considered as they will determine the reliability of the whole system. If the devices are not equally stressed, one device will degrade at a faster rate than another. The electrothermal simulations as well as finite element (FE) simulations are used to investigate the electrothermal stresses between series connected devices under balanced and unbalanced conditions. This thesis covers the following aspects:

(i) Characterisation of the voltage sharing between series connected devices during ON-state, OFF-state and transient switching. To connect devices in

series to develop high voltage capability of the whole system is very important for high voltage applications. The semiconductor physics of these devices is used to understand the nature of voltage sharing for different technologies.

(ii) Loss of gate drive synchronization or variation in device switching time constant can cause voltage imbalance between the series devices. This uncontrolled voltage imbalance can have destructive consequences as it takes device into avalanche mode conduction. By introducing delays between the gate drivers at different switching speeds and different DC link voltages, correlations have been established between the maximum gate trigger mismatch and electrothermal failure under dynamic avalanche. This information is important for power electronics engineers designing active gate controllers for series connected power devices because it defines the boundary conditions for the bandwidth of the controllers. Experimental measurements and simulations have been used to investigate the limits of the power devices under dynamic avalanche as a function of the switching speed and the operational voltage.

(iii) In multilevel inverters or MMC one device module might contain few devices connected in series. Therefore it is important to know the electrothermal stresses within the inverter, since in the 3L-NPC converter, depending on the application, the devices are not equally stressed, hence, lthe lifetime of the converter is dependent on the lifetime of the most

stressed power device within it. A compact electrical drive model coupled with an electro-thermal power electronic model was developed in MATLAB/Simulink and used for driving a permanent magnet synchronous motor through a 3L-NPC inverter and experimental measurements were completed for better understanding the distribution of electrothermal stresses within the inverter.

1.4 Overview of the thesis

Chapter 2 provides a brief introduction to the series connected devices of different device types for high voltage applications. This section of the thesis focuses on the applications of series connected devices. A brief introduction to multilevel converters is provided and the summary of 3-level Neutral Point Clamped inverter is discussed. Moreover, the intrinsic problem of voltage sharing of series connected devices was discussed and the advantages and disadvantages of the methods to prevent the voltage unbalance were analysed.

Chapter 3 presents the results of static on-state and off-state voltage sharing in series connected power devices. The chapter gives the detailed introduction to the physics of power devices (SiC MOSFET, SiC Schottky diodes, Si IGBT, Si PiN diodes) under on and off state conditions. Moreover, a compact electrothermal model of two series connected power devices is provided and simulation results of voltage sharing of series

connected power devices during the ON-state are presented. The results of this chapter have been reviewed, accepted and presented as conference publication in IEEE 8th International Power Electronics Conference and ECCE Asia (IPEC 2018 - ECCE Asia) in Niigata 2018.

Chapter 4 presents the results of dynamic voltage sharing in series connected devices. The chapter starts with the introduction of the physics of power devices during turn-off. The impact of variation in the initial junction temperature and switching speeds between the series connected devices have been investigated for different technologies. This is supported by FE simulations that give deep understanding of the internal physics of the device through the electric field and carrier concentration graphs. Moreover, a compact model that predicts voltage divergence between mismatched series connected power devices by using datasheet parameters like leakage currents and output capacitances has been developed in Matlab/Simulink. The analysis, modelling and experimental results of this chapter have been presented in IEEE International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe 2018) in Nuremberg in 2018. Also the FE simulation results will be presented in the IEEE European Power Electronics (EPE) conference in Riga 2018.

Chapter 5 provides the experimental measurements and FE simulations that have been used to investigate the SOA of series connected silicon field-stop IGBTs and SiC Trench MOSFETs. This chapter investigates the performance of series connected SiC power MOSFETs and silicon IGBTs under dynamic avalanche conditions. By introducing

delays between the gate drivers at different switching speeds and different DC link voltages, correlations have been established between the maximum gate trigger mismatch (between the series pair) and electrothermal failure under dynamic avalanche. The results of this chapter have been reviewed, critiqued and accepted as conference publication and will be presented in IEEE 10th Annual Energy Conversion Congress and Exposition (ECCE 2018) in Portland.

Chapter 6 presents a compact electrical drive model coupled with an electro-thermal power electronic model that is used for driving a PMSM through a 3L-NPC inverter. The experimental results to analyse the electrothermal stresses within the inverter and impact of different power factors have been obtained from H-bridge 3-level NPC inverter which was built for the purpose of these experiments. The method, analysis and results of this chapter have been published as conference paper and presented in IEEE International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe 2017) in Nuremberg in 2017.

Chapter 7 concludes the thesis and proposes some further work which would be beneficial for further investigation of series connection of power devices.

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Chapter

2 Introduction to Series Connected Devices

2.1 Introduction

The first advent of power electronics in grid applications like HVDC were line commutated current source converters based on series connected thyristor valves [39]. The converters were current sourced because the DC side current was constant and the polarity of the DC side voltage determined the direction of power flow. The firing angle of the thyristor was used to determine the operational mode of the converter. The converters were line commutated because the phase-to-phase current commutation was initiated by the system AC voltage reversal. Using phase controlled thyristors usually in pressure-packages, high power line-commutated converters (LCC) systems were implemented with bi-directional power flow capability. One limitation however, with LCC systems is the inability to synthesize 3-phase AC voltages, hence, LCC systems

need strong synchronous AC systems on both sides of the converter [40] i.e. LCC systems cannot black-start. In high power motor drive applications like rail traction, DC motor drives were implemented with current source converters. However, there were limitations in LCC systems that led to the development of self-commutated Voltage Source Converters (VSCs). VSCs are voltage sourced because the DC side voltage is constant and the direction of power flow is determined by the polarity of the DC side current. The VSC inverts when the transistors conduct and rectifies when the diodes conduct. Fig.2.1 (a) shows a 6-pulse line commutated current source converter (CSC) while Fig.2.1 (b) shows a 3-phase 2-level VSC. The LCC system shown is a 6-pulse converter because there are 6 commutations per cycle corresponding to the 6 devices. To reduce the DC side voltage harmonics, two 6-pulse LC-CSCs can be cascaded to form a 12-pulse converter. To achieve, this, a 30° phase shift is introduced between the 2 converters by using a transformer with a star primary and a delta secondary.

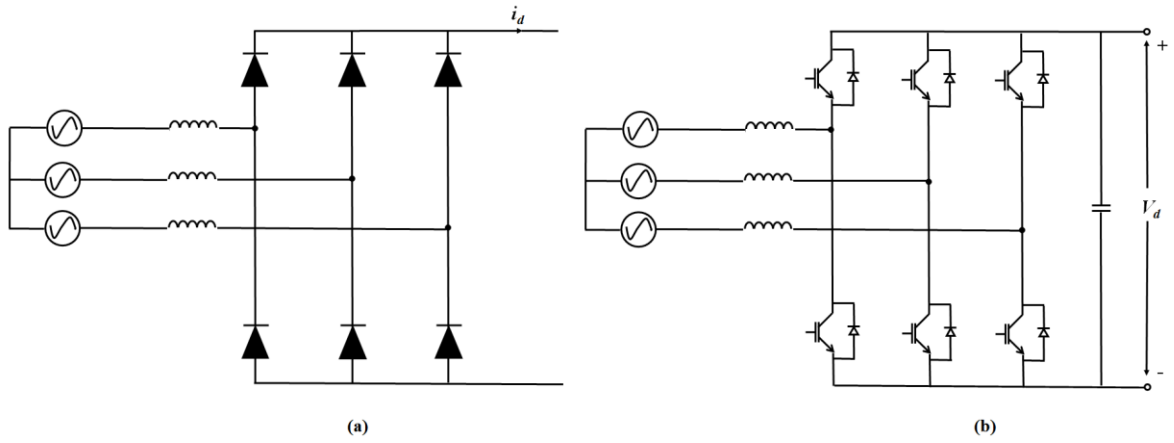

Fig. 2.1 (a) 6-pulse line commutated current source converter and (b) a 3-phase 2-level voltage source converter.

Unlike LCC systems, VSCs are capable of 4-quadrant operation i.e. rectify and invert at leading and lagging power factor. The earliest VSCs were 2 level 3-phase VSCs for motor drive applications, however, as high voltage IGBTs were developed, the VSC was scaled up in power handling capability. Unlike thyristors, IGBTs are capable of self-turn OFF. Thyristors are 4-layer PNPN devices that conduct current through avalanche multiplication. Fig. 2.2 shows the schematic diagram of a thyristor showing how it is comprised to two cross-coupled BJTs (one NPN and one PNP) with the collector of each transistor connected to the base of the other transistor. When thyristors conduct current, an intermediate PN junction is broken down and current flows through impact ionization. The collector current of the NPN BJT feeds into the base current of the PNP BJT and vice-versa. Hence, the thyristor is said to latch when both BJTs are ON and mutually reinforcing one another. Thyristors are capable of very high conduction current since entire 6-inch wafers can be configured to conduct current through the bulk.

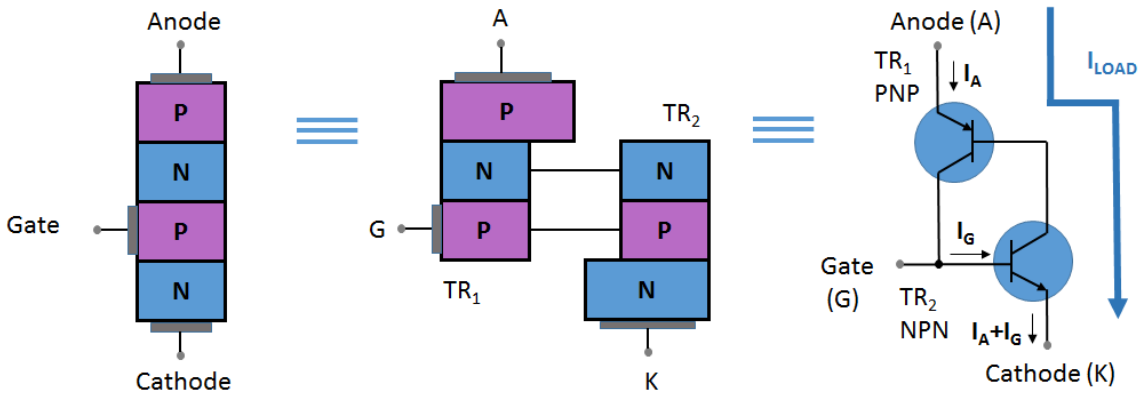

Fig. 2.2 Schematic of a thyristor showing the internal junctions and BJTs.

However, the thyristors can only be turned OFF either by reducing the current through the thyristor to below the holding current or by reversing the voltage across the terminals of the thyristor. IGBTs however are MOS controlled BJTs with a MOS channel that can be very finely controlled by a gate driver. Hence, by designing a switching pattern with high switching frequencies, IGBT based VSCs are capable of synthesizing 3-phase AC voltages without requiring an existing AC system i.e. VSCs are capable of black-starting. This also means VSCs can have reduced filtering requirements since they are capable of higher switching frequencies thereby moving the high-power harmonics to higher frequencies.

The earliest high-power voltage source converters for HVDC applications were 2-level converters with series connected devices for static and dynamic voltage balancing. This converter, developed by ABB [41], was implemented with PWM hence, the high dV/dts resulting from switching the high DC voltage at high frequencies caused considerable electromagnetic stresses. Furthermore, the high switching losses made this converter uncompetitive compared to the LCC system. Later developments resulted in multi-level converters including flying capacitor converters [42], diode clamped converters [7] and cascaded H-bridge converters [43]. The basic idea behind the multi-level converter is to synthesize the AC voltage waveform by using a large number of DC sources switched in as voltage steps. Hence, the larger the number of steps/levels, the smoother the AC waveform and the less harmonic filtering is required. However, this would be at the cost of increased complexity in converter control since there are numerous DC sources (usually capacitors) that must be controlled. Fig. 2.3

shows the output phase voltage waveforms of a 2-level converter compared to that of a 3 level converter. By comparing both waveforms, it can be seen that the 3L converter has more voltage steps in the phase voltage waveform.

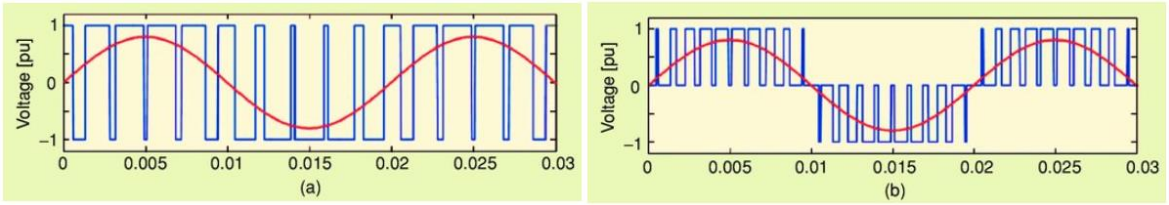

Fig. 2.3 Output phase voltage waveforms: (a) two-level inverter (b) three-level inverter [44].

2.2 Summary of Three-level Converter Operation

The NPC inverter was introduced by Nabae, Takahashi, and Akagi in 1981, also known as diode-clamped converter [7]. It became the most widely used topology in different industrial applications. This sub-chapter presents a general description of common features and developments of this topology modulation strategies, loss performance as well as control methods and use of power devices.

The three-level NPC converter is an increasingly popular topology for medium voltage industrial AC drives, wind energy conversion systems and grid connected converters. Fig. 2.4 shows the circuit of the three-level neutral-point clamped inverter. The DC bus voltage is divided into three levels by two-series connected capacitors, C1 and C2. The middle voltage level N of the two capacitors can be defined as neutral point

level. The output voltage of each 3-phase (V_a, V_b, V_c) has three states: $V_{dc}/2$, 0 and - $V_{dc}/2$. For voltage level $V_{dc}/2$ transistors T1 and T2 need to be switched ON, for - $V_{dc}/2$ level, transistors T3 and T4 need to be switched ON; and for 0 level , T2 and T3 have to be ON. Table 2.1 presents the transistor conduction states for phase A. The diodes CD1 and CD2 clamp the transistor voltage to half the level of the DC-bus voltage.

Table 2.1 Three-level Switching States

Output Voltage, V_a	**Transistor states**			
	T1	**T2**	**T3**	**T4**
$V_{dc}/2$	1	1	0	0
0	0	1	1	0
- $V_{dc}/2$	0	0	1	1

The switching strategy used typically can be square-wave excitation, sinusoidal pulse width modulation (SPWM) or space-vector pulse width modulation (SVPWM).There are three main methods to generate the desired converter voltage by three-level inverter. These modulation schemes are as follows: 1) carrier-based sine-triangle modulation; 2) space vector modulation (SVM); 3) selective harmonic elimination (SHE).

Carrier-based 3-level PWM modulation is highly applied modulation methods in the industry [17, 18], which is based on the comparison of a sinusoidal reference voltage with two carriers. There is a continuous research on this modulation method in terms

of optimal switching sequences [17], different modulation indexes [19], new topologies [20] and etc.

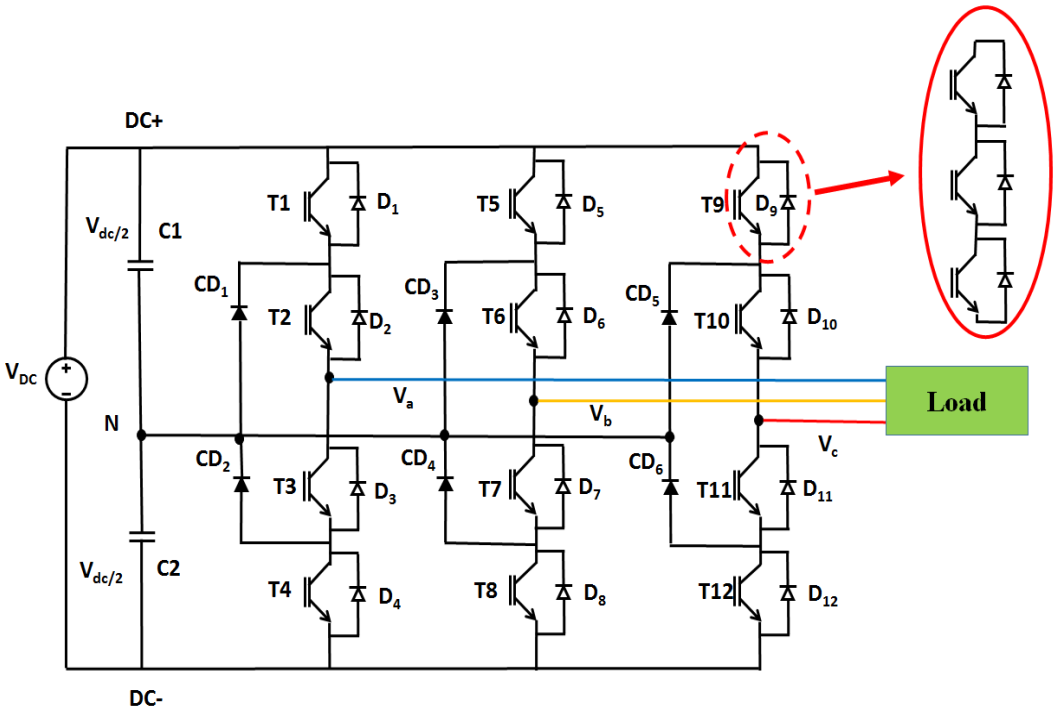

Fig. 2.4 Circuit schematic of the three-level neutral-point clamped inverter.

In 3-level NPC inverter each switching device can comprise multiple series connected devices as it shown in Fig.2.4. Therefore it is important to know the electrothermal stresses within the inverter, since the in the 3L-NPC converter, depending on the application, the devices are not equally stressed, hence, the lifetime of the converter is dependent on the lifetime of the most stressed power device within it. Therefore, there is increasing focus on the thermal stresses and power loss distribution on the devices within the 3L-NPC converter [35].

2.3 Voltage Sharing in Series Connected Devices

In high voltage applications such as switching-mode power supply and DC-circuit breaker [2, 21], high blocking voltage capability of the switching power electronic devices are needed. As explained earlier, for such applications, series connection of the IGBTs and more recently with emerging of wide bandgap semiconductors, SiC MOSFETs are required [3, 4]. The intrinsic problem with series connected devices is the voltage sharing between the devices which leads to unbalance electro-thermal stress on the devices. As mentioned earlier, the unbalance voltage sharing can be a consequence of variation in the internal structure of the device and the manufacturing tolerances of the dies which is inevitable. The variations of the physical parameters of the devices which can lead to unbalanced voltage sharing are slight differences in the leakage current, carrier lifetime in the drift region, doping of the drift region, mobility of the carriers, threshold voltage and presence of defects on the crystal lattice (more applicable to SiC crystalline structure) [22-25]. In addition, differences in the circuit layout and different spread of electrical circuit parameters as well as non-uniform gate driver circuit leads to this unbalance voltage sharing.

Several methods have been implemented to reduce the undesired unbalance voltage sharing between the devices such as: (i) adding external passive snubber; (ii) implementing an active clamping circuits; (iii) introducing delay time in switching of

the series connected devices; and (iv) using active gate drive control. These methods have been investigated and analysed in several different publications ([26-34]), however, in none of these works, the impact of temperature imbalance, switching rate imbalance and the impact of using different power switching technology is not investigated. These are very important to understand the details of dynamic and switching voltage unbalancing specially for active drive control method where the snubber and external circuitry will not be used.

Adding an external passive snubber is an effective way to balance the voltage sharing [26], however, this is only useful during the off-state of the transistors and during the switching, this introduces additional losses as the snubber slows down the switching transient. In addition, this method increases the part count number as well as increases the weight and cost of the system. Active clamping circuits also increase the cost of the system and reduces the reliability of the device as it requires additional circuitry (Zener diodes to clamp the collector-emitter voltage) for each switching device [36]. In addition, active clamping circuits require current feedback to the gate to enable slight turn-on of the device when overvoltage occurs. Additional external resistors and capacitors are also added to the circuit to improve the balancing performance. This method was originally used as a measure of overvoltage and is not particularly useful for static voltage balancing and to improve this, an additional status feedback circuit needs to be implemented to improve the voltage balancing [29]. Overall, this method is complex and costly.

Introducing delay in the gate signal [34] can be done if each device has a separate gate drive circuit with separate voltage supply to balance the switching speed of the devices to achieve a balance voltage sharing but it is not particularly useful if the voltage imbalance is due to dV/dt difference between the switching of the devices. The dV/dt differences can be due to difference in the operating temperature, gate resistance, carrier lifetime (in case of bipolar devices) and background doping of the device.

In active gate drive control method [37, 38], the gate current is controlled to achieve a desirable voltage waveform. The complexity of this method increases as the number of series connected devices are increased. This method requires a state detection circuit, optical couplers, FPGA controller and a current source drive which is controlled by the FPGA for each switching device.

Gate drive circuits are supposed to provide facilities to switch on and off the power device and to control and protect it under different load and fault conditions. The gate driver should reduce the over-voltage and over-current problems without harmful effect on the efficiency. The basic concept of the active gate drivers is the modification of the gate-source voltage slope in two stages using a simple closed-loop control [45].

Gate drive circuits are primarily used to provide gate signals to control the switching of gate-controlled power devices. As the system becomes more complex and as the functionality of the inverter becomes crucial in the safety of the system, the functional safety concepts require the power converter to put additional control for fault detection and converter shutdown or de-rate under different conditions. Recently, the gate driver boards are also responsible for controlling the over voltage, over current,

under voltage, under current, desaturation, thermal de-rate, voltage clamping, switching frequency change to enhance the efficiency and improving the switching and ringing losses by modulating a complex waveform on the gate of the device and many other non-functional safety features. This is mainly due to the fact that the gate driver, is the closest component to the active high voltage device that can control the power flow at the lowest level.

As the power demand increases and converter topologies become more complex (possibly the number of levels used on the converter increases on many medium and high voltage applications), the need of controlling the devices, synchronising the switching effects on the series and parallel connected devices and making the converter fail-safe becomes more crucial.

The Active Gate Drivers add control to the power of the driving signal which means more parameters would be controlled actively during the operation of the power converter; namely, the switching time or waveform time. This would require a very enhanced gate driver circuit which in return allows exploration of advanced features of wide band gap semiconductors which can switch at a significantly faster rate than the conventional devices. Since the active gate drivers also determine the losses and have important effects on the system performance including the reliability and efficiency. Active thermal control techniques can also be implemented using specialized gate drivers and even embedded state of the art measurements for on-board diagnostics can also be implemented using active gate control.

The active gate driver should also provide electrical insulation among devices and circuit components, limiting damage in case of failure of power lines or hardware. Limiting dv/dt and di/dt to control the harmonic content of the generated waveform is desired, as well as EMI control [46].

The active gate driver can also provide electrical insulation among devices and circuit components, limiting propagation of damage in case of failure of power lines or hardware. In addition, active gate driver can control the harmonic content of the generated waveform to desired values as well as controlling the EMI through actively controlling the switching rate (dV/dt and dI/dt).

As the switching frequency of SiC MOSFETs are significantly higher than conventional IGBTs, the active gate driver concept becomes increasingly interesting when it comes to load balancing between series and parallel connected devices as the voltage and current sharing can be controlled precisely through a closed-loop control on the gate signal waveform.

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Chapter

3 Static ON-State and OFF-State Voltage Sharing in Series Connected Power Devices

3.1 Introduction

Series connected power devices are required for voltage sharing in high voltage applications like grid connected converters [1, 8, 9]. With SiC considered as a strong contender for grid applications, the performance and reliability issues associated with voltage sharing compared to contemporary silicon bipolar devices is important to consider [2]. In applications where series power devices may be at different junction temperatures as a result of the physical architecture of the converter cooling system or differential degradation of the packaging, the zero-temperature coefficient of the power devices determines the voltage sharing and loss distribution in the ON-state while the leakage current and switching synchronization is critical in the OFF-state. In the ON-state, the lower zero-temperature-coefficient (ZTC) point in SiC devices contributes to

increasing voltage divergence with the higher thermal resistance device increasingly dissipating more power. In this case, the higher ZTC point in silicon bipolar devices is an advantage although it is a disadvantage for paralleling.

3.2 Temperature dependence of I-V characteristics

3.2.1 Series SiC MOSFET in ON-State

The SiC MOSFET is increasingly becoming the main competitor of the silicon IGBT in low to medium voltage applications. The drain current of the MOSFET can be derived from first principles using Fig.3.1 below as a reference. Assuming a volume of charge (At_i) containing n carriers per unit cm^{-3}. The volume of charge has length L and width W. The volume of charge is formed in a p-doped layer and is full of mobile electrons connecting an n-doped source terminal to another n-doped drain terminal. The volume of charge is inverted from a majority p-doped layer into an n-doped layer by applying a voltage across the gate that exceeds the threshold voltage of the MOSFET. The threshold voltage of the MOSFET is given by the sum of the flatband voltage, the voltage across the gate dielectric and the surface potential of the MOSFET [3, 4], equation 3.1.

$$V_{TH} = V_{FB} + \varphi_s + V_{OX} \quad (3.1)$$

The equation 3.1 can be rewritten as:

$$V_{TH} = \left(\phi_{ms} - \frac{Q_f}{C_{OX}}\right) + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) + \frac{1}{C_{OX}}\sqrt{4\varepsilon_{si}qN_A\frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)} \quad (3.2)$$

where C_{OX} is the thickness of the gate oxide, ϕ_{ms} is work function, Q_f is fixed oxide charge, ε_{si} is the semiconductor dielectric constant, k is the Boltzmann's constant, N_A is the doping concentration in the p-base region and n_i is the intrinsic carrier concentration.

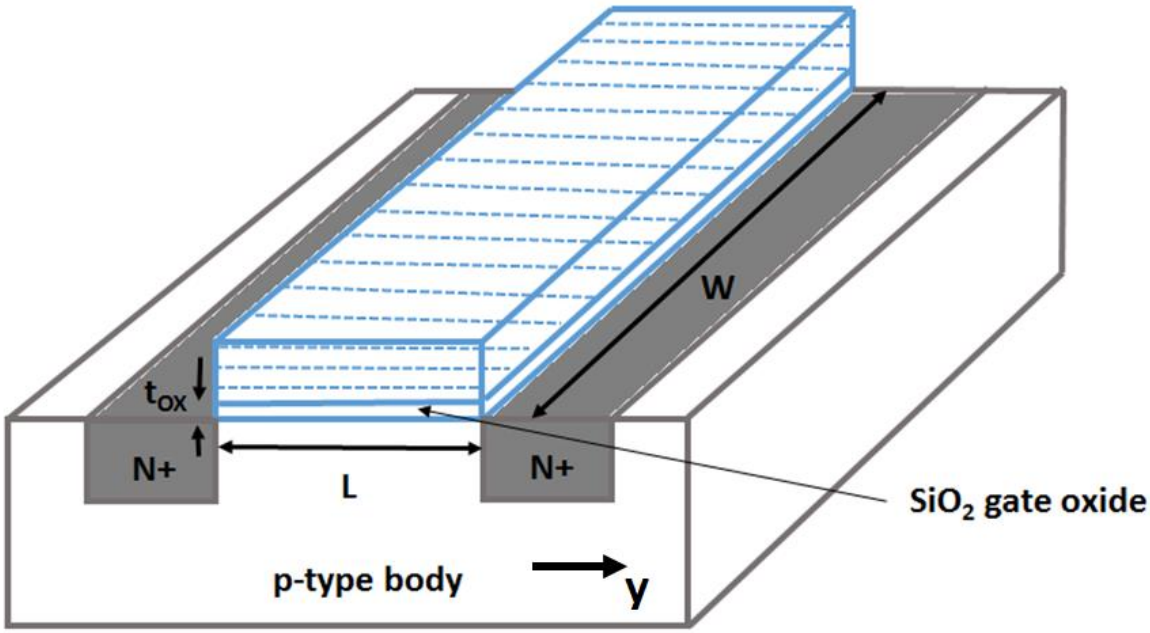

Fig. 3.1 Schematic of the MOSFET Structure.

$$I = \frac{Q}{t} = \frac{nqA}{L} v_d \tag{3.3}$$

where $v_d = \mu E$ is the drift velocity defined by the product of the effective mobility (μ) and lateral electric field (E) in the direction of the current flow.

$$I = \frac{nqA\mu E}{L} \tag{3.4}$$

The volume of the charge can be assumed to be equal to a sheet of charge according to the charge sheet approximation [16-18].

$$nq = C_{OX}(V_{GS} - V_{th} - V_y) \tag{3.5}$$

$$I = \frac{WLC_{OX}(V_{GS} - V_{th} - V_y)\mu E}{L} \tag{3.6}$$

$$I = W\mu C_{OX}(V_{GS} - V_{th} - V_y)\frac{dV}{dy} \tag{3.7}$$

$$\int_0^L I dy = W\mu C_{OX}\int_0^{V_{DS}} (V_{GS} - V_{th} - V_y) dV \tag{3.8}$$

The drain current can be solved by integrating the voltage in the direction of the lateral electric field [17].

$$I = \frac{W\mu C_{OX}}{L}\left((V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right) \tag{3.9}$$

When the drain voltage of the MOSFET is increased, the channel becomes pinched OFF and the MOSFET goes into saturation. When this happens, the drain current becomes independent of the drain voltage. In saturation, $V_{DS}=V_{GS}-V_{TH}$

$$I_{DS} = \frac{W\mu C_{OX}}{2L}(V_{GS} - V_{TH})^2 \tag{3.10}$$

In the ohmic region, the ON-state voltage is small, hence, equation 3.8 can be re-written as:

$$I_{DS} = \frac{W\mu C_{OX}}{L}(V_{GS} - V_{TH})V_{DS} \tag{3.11}$$

Fig. 3.2 shows idealised gate transfer and output characteristics of a MOSFET

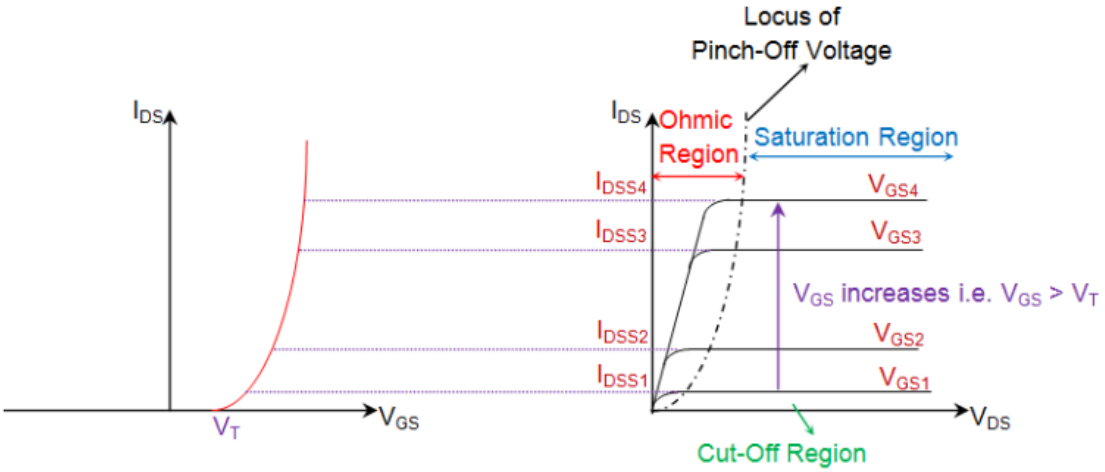

Fig. 3.2 Idealised gate transfer and output characteristics of a MOSFET [25].

The channel resistance (R_{CH}) of the channel can be derived as:

$$R_{CH} = \frac{V_{DS}}{I_{DS}} = \frac{L}{W\mu C_{OX}(V_{GS} - V_{TH})} \tag{3.12}$$

The derivative of the channel resistance with respect to temperature is given by

$$\frac{dR_{CH}}{dT} = \frac{L}{WC_{OX}} \frac{d}{dT}\left(\frac{1}{\mu(V_{GS} - V_{TH})}\right) \tag{3.13}$$

$$\frac{dR_{CH}}{dT} = \frac{L}{WC_{OX}\left(\mu(V_{GS} - V_{TH})\right)^2}\left(\mu\frac{dV_{TH}}{dT} - (V_{GS} - V_{TH})\frac{d\mu}{dT}\right) \tag{3.14}$$

Close observation of equation 3.14 shows that there are 2 competing mechanisms that determines the temperature coefficient of the channel resistance. These are the effective mobility and the threshold voltage. The effective mobility reduces with increasing temperatures. This relationship can be derived from the basis that the electric field that produces a force on the unit charge can be defined as the force per unit charge and the force is simply the product of the mass of the charge and its acceleration [16-18].

$$F = qE = ma \tag{3.15}$$

$$a = \frac{qE}{m} \tag{3.16}$$

$$v_d = \int a.dt = \frac{qE}{m}\tau \tag{3.17}$$

$$v_d = \frac{q\tau}{m}E = \mu E \quad \text{where} \quad \mu = \frac{q\tau}{m} \tag{3.18}$$

In equation 3.18 above, τ is the electron scattering relaxation time i.e. the time between scattering events between electrons and other electrons, ionized dopants and traps.

High temperature reduces the scattering relaxation time by reducing the electron mean free path (the distance the electron travels between scattering events). This process is known as acoustic phonon scattering and is simply characterised by atomic vibrations that increase with temperature. For electrons in silicon and SiC, the temperature dependency of the effective mobility is given empirically by:

$$\mu = 1360\left(\frac{T}{300}\right)^{-2.42} \quad \text{and} \quad \mu = 1140\left(\frac{T}{300}\right)^{-2.7} \tag{3.19}$$

The threshold voltage also reduces with temperature due to an increase in the intrinsic carrier concentration i.e. electron hole pair generation rates increase with temperature. The threshold voltage in equation in 3.2 can be re-written as:

$$V_{TH} = \left(\phi_{ms} - \frac{Q_f}{C_{OX}}\right) + 2\phi_B + \frac{1}{C_{OX}}\sqrt{4\varepsilon_{si} q N_A \phi_B} \tag{3.20}$$

where is ϕ_B the bulk potential which depends on the p-body doping. The temperature dependency of the threshold voltage is given by:

$$\frac{dV_{TH}}{dT} = \frac{d\phi_B}{dT}\left(2 + \frac{1}{C_{OX}}\sqrt{\frac{q\varepsilon N_A}{\phi_B}}\right) \tag{3.21}$$

As temperature increases, the threshold voltage reduces thereby reducing the channel resistance according to equation 3.20. However, the effective mobility will also reduce thereby increasing the channel resistance. The temperature coefficient of the channel resistance is usually negative because the reduction of the threshold voltage usually overcomes the reduction of the effective mobility. Hence, the channel resistance reduces

with increasing temperature as a result of the increase in the carrier concentration in the channel.

The total resistance of the MOSFET in the ON-state will be a series combination of the source resistance, channel resistance, accumulation resistance, drift resistance, substrate resistance and metal contact resistances. However, the two major components are the channel resistance and the drift resistance. The drift resistance of the MOSFET dominates the total resistance as the voltage blocking capability of the MOSFET is high since thicker and more resistance epitaxial layers are needed to block higher voltages. The drift resistance and its temperature dependency is given by [3,4]

$$R_{drift} = \frac{4B_{VD}^2}{\varepsilon_{si}\mu E_C^3} \quad \text{and} \quad \frac{dR_{drift}}{dT} = \frac{4B_{VD}^2}{\varepsilon_{si}E_C^3}\frac{d}{dT}\left(\frac{1}{\mu}\right) \tag{3.22}$$

The temperature coefficient of the drift resistance is always positive because of the temperature dependency of the effective mobility as discussed earlier (drift resistance increases with increasing temperature due to a reduction of the effective mobility). Hence the total ON-state resistance (comprising of both the drift resistance and the channel resistance) of the MOSFET will exhibit a temperature dependency that depends on the relative proportions of the channel resistance and the drift resistance. If the channel resistance is the dominant factor, then the ON-state resistance will reduce with temperature. However, if the drift resistance is the dominant factor, then the total resistance will increase with temperature. The equations shown below model the temperature dependency of the total ON-state resistance as follows:

$$R_{DS} = \frac{L}{W\mu C_{OX}\left(V_{GS} - V_{TH}\right)} + \frac{4B_{VD}^2}{\varepsilon_s \mu E_C^3} \tag{3.23}$$

$$\frac{dR_{DS}}{dT} = \frac{dR_{CH}}{dT} + \frac{dR_{drift}}{dT} \tag{3.24}$$

$$\frac{dR_{DS}}{dT} = \left(\frac{L}{WC_{OX}\left(\mu(V_{GS} - V_{TH})\right)^2} \left(\mu \left| \frac{dV_{TH}}{dT} \right| \right) - \left(V_{GS} - V_{TH}\right) \left| \frac{d\mu}{dT} \right| \right) + \frac{4B_{VD}^2}{\varepsilon_s E_c^3} \frac{d}{dT}\left(\frac{1}{\mu}\right) \tag{3.25}$$

$$\frac{dR_{DS}}{dT} = \frac{L\mu \left| \frac{dV_{TH}}{dT} \right|}{WC_{OX}\left(\mu(V_{GS} - V_{TH})\right)^2} - \frac{4B_{VD}^2}{\varepsilon_s E_c^3 \mu^2} \left| \frac{d\mu}{dT} \right| \tag{3.26}$$

In deriving equation 3.26, it is assumed that the temperature dependency of the effective mobility (especially in SiC MOSFETs) is much smaller than the temperature dependency of the threshold voltage. Shown below is the temperature dependency of the ON-state resistance in CREE's latest generation 1.2 kV SiC MOSFET.

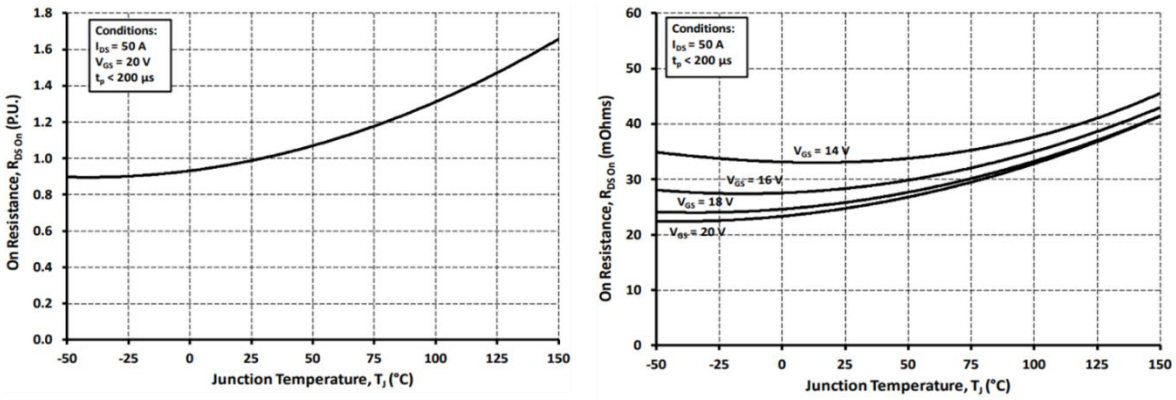

Fig. 3.3 On-state resistance vs temperature at the recommended gate drive voltage and other voltages.

As can be seen from Fig. 3.3 [6], the total ON-resistance increases with temperature at the recommended gate drive voltage (which is 20 V), however, as the gate voltage is reduced, the temperature dependency becomes more monotonic because the channel becomes a more dominant factor in the total ON-state resistance. However, the important consideration to note is that the temperature coefficient of the ON-state resistance is always positive as long as the MOSFET is driven at its recommended gate drive voltage.

When the power MOSFET is used in a power converter, the current through the MOSFET depends on the load the converter is driving. Hence, the MOSFET can be represented as an ON-state resistance which depends on the device technology. The MOSFET will be an electrothermal system, which means that the electrical properties (conduction and switching losses) will determine the junction temperature through the thermal resistance (junction-to-case and case-to-ambient thermal resistances) since the temperature is the ratio of the thermal resistance to the instantaneous power. The junction temperature in-turn determines the electrical properties, like the threshold voltage, effective mobility etc. Hence, it is a coupled electrical and thermal system.

Fig.3.4 shows the simulated forward and transfer characteristics of SiC MOSFET.

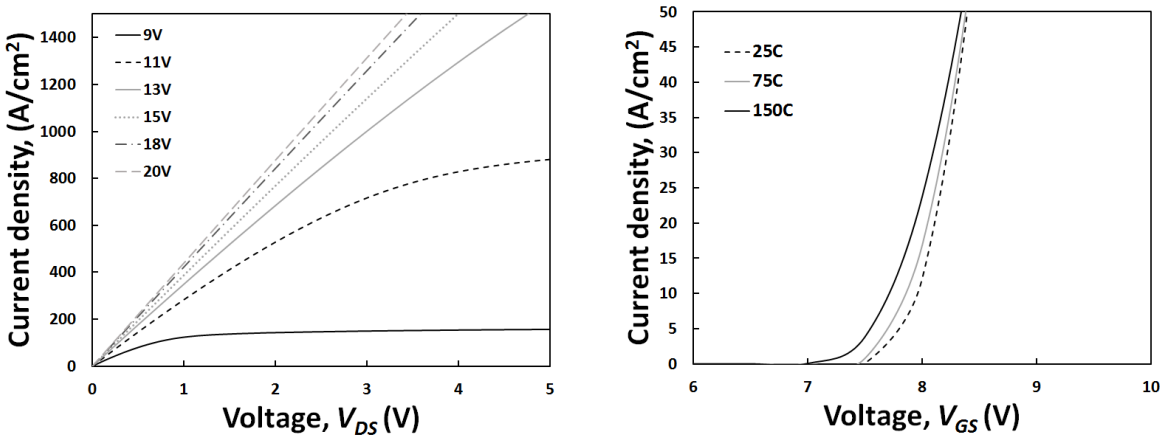

Fig. 3.4 Simulated forward and transfer characteristics of the SiC Trench MOSFET.

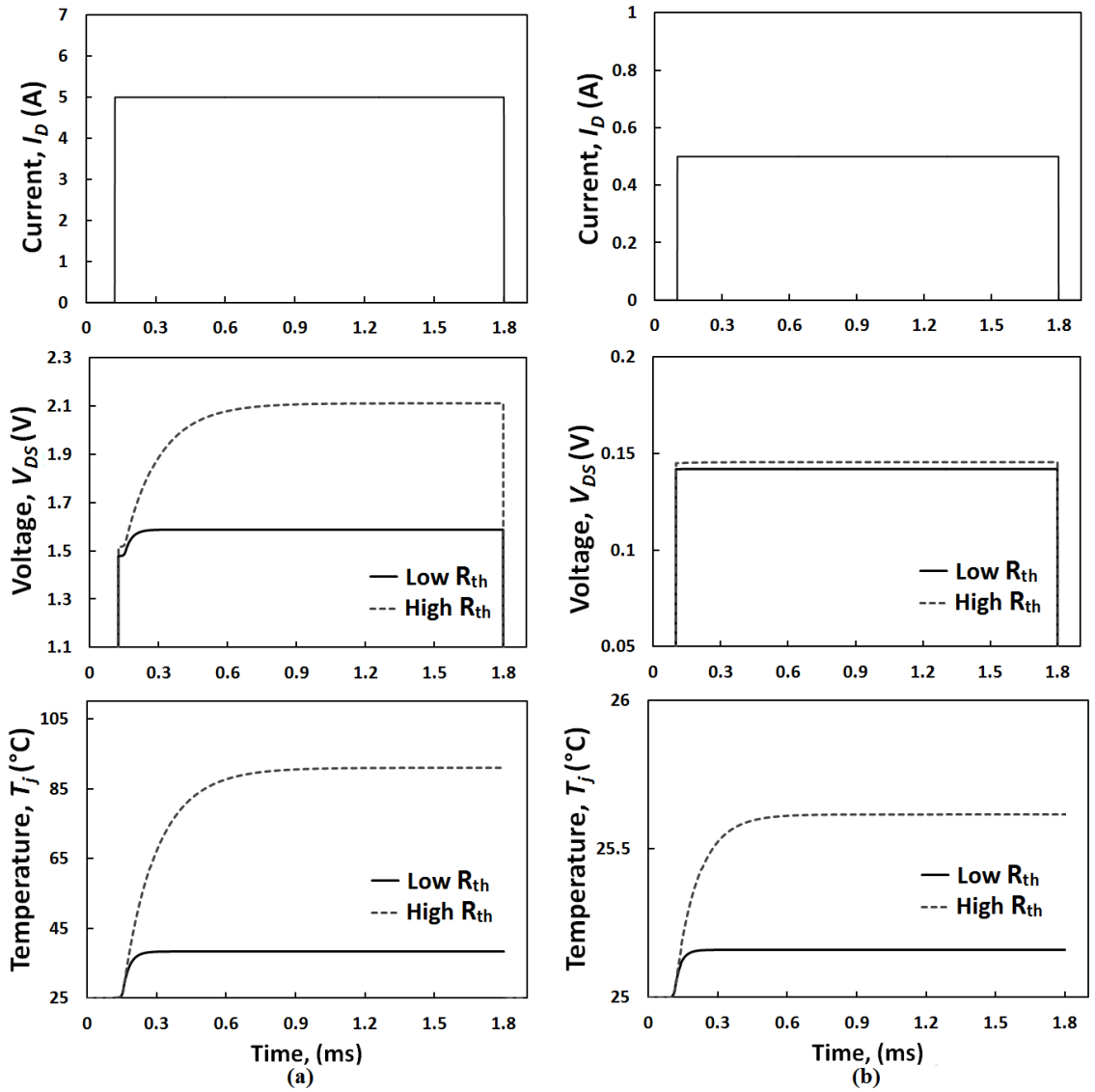

Fig. 3.5 Simulated I_{DS}, V_{DS} and Junction Temperature characteristics of the series connected SiC MOSFETs for different current levels a) 5A b) 0.5A above the ZTC point.

Fig.3.5 (a) and (b) shows the simulated characteristics of the series connected SiC MOSFETs for different current levels for current of 5A and 0.5A above ZTC point respectively.

3.2.2 Series SiC Schottky Diodes

The forward voltage in a Schottky Barrier Diode (SBD) is given by [3-5, 19]:

$$V_F = \frac{kT}{q}\ln\left(\frac{J_F}{J_S}\right) + J_F R_S \tag{3.27}$$

where J_F is the forward current density, J_S is the saturation current density and R_S is the parasitic series resistance. The saturation current density is dependent on temperature and Schottky barrier height according to [3]:

$$J_S = AT^2 e^{-\frac{q\phi_{BN}}{kT}} \tag{3.28}$$

The temperature derivative of the forward voltage is given by:

$$\frac{dV_F}{dT} = J_F\frac{dR_S}{dT} + \frac{k}{q}\ln\left(\frac{J_F}{J_S}\right) - \frac{kT}{q}\frac{1}{J_S}\frac{dJ_S}{dT} \tag{3.29}$$

where the temperature dependency of the saturation current is given by:

$$\frac{dJ_S}{dT} = Ae^{-\frac{q\phi_{BN}}{kT}}\left(\frac{q\phi_{BN}}{k} + 2T\right) \tag{3.30}$$

The zero temperature coefficient current for the SiC Schottky diode can be calculated by setting the temperature derivative in (3.29) to zero and determining the forward current.

$$J_F\frac{dR_S}{dT} + \frac{k}{q}\ln\left(\frac{J_F}{J_S}\right) = \left(\frac{q\phi_{BN}}{k} + 2T\right)\frac{kT}{q}\frac{1}{J_S^2}Ae^{-\frac{q\phi_{BN}}{kT}} \tag{3.31}$$

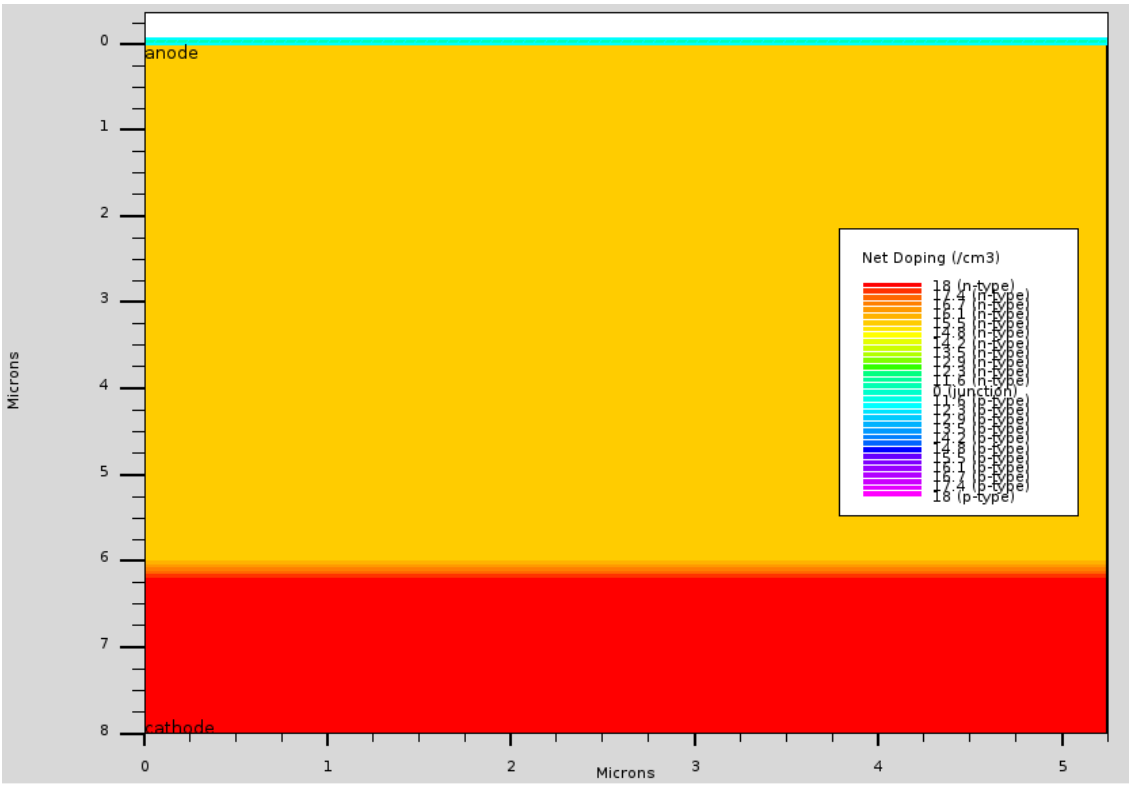

Fig. 3.6 SiC Schottky diode model rated at 600V.

Fig.3.6 shows an example of a finite element simulated 600V SiC Schottky diode with a drift layer thickness of 6 μm and n-type doping level of 1.1×10^{16} cm^{-3}. Fig.3.7 shows the simulated forward and reverse characteristics of the SiC SBD using FE modelling.

Fig.3.8 (a) and (b) shows the simulated characteristics of the series connected SiC Schottky diodes for different current levels for current of 4A and 1A above ZTC point respectively.

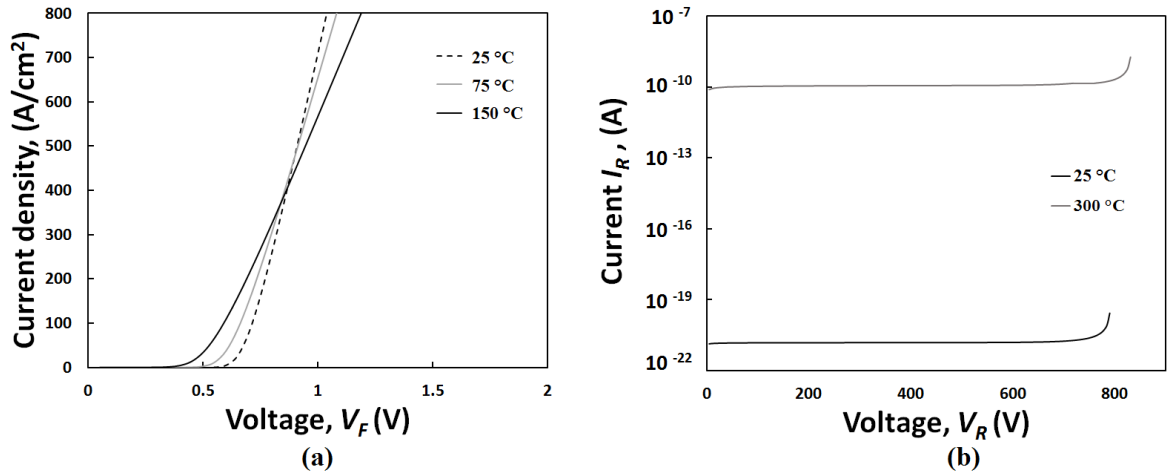

Fig. 3.7 Simulated forward and reverse characteristics of the SiC Schottky diode.

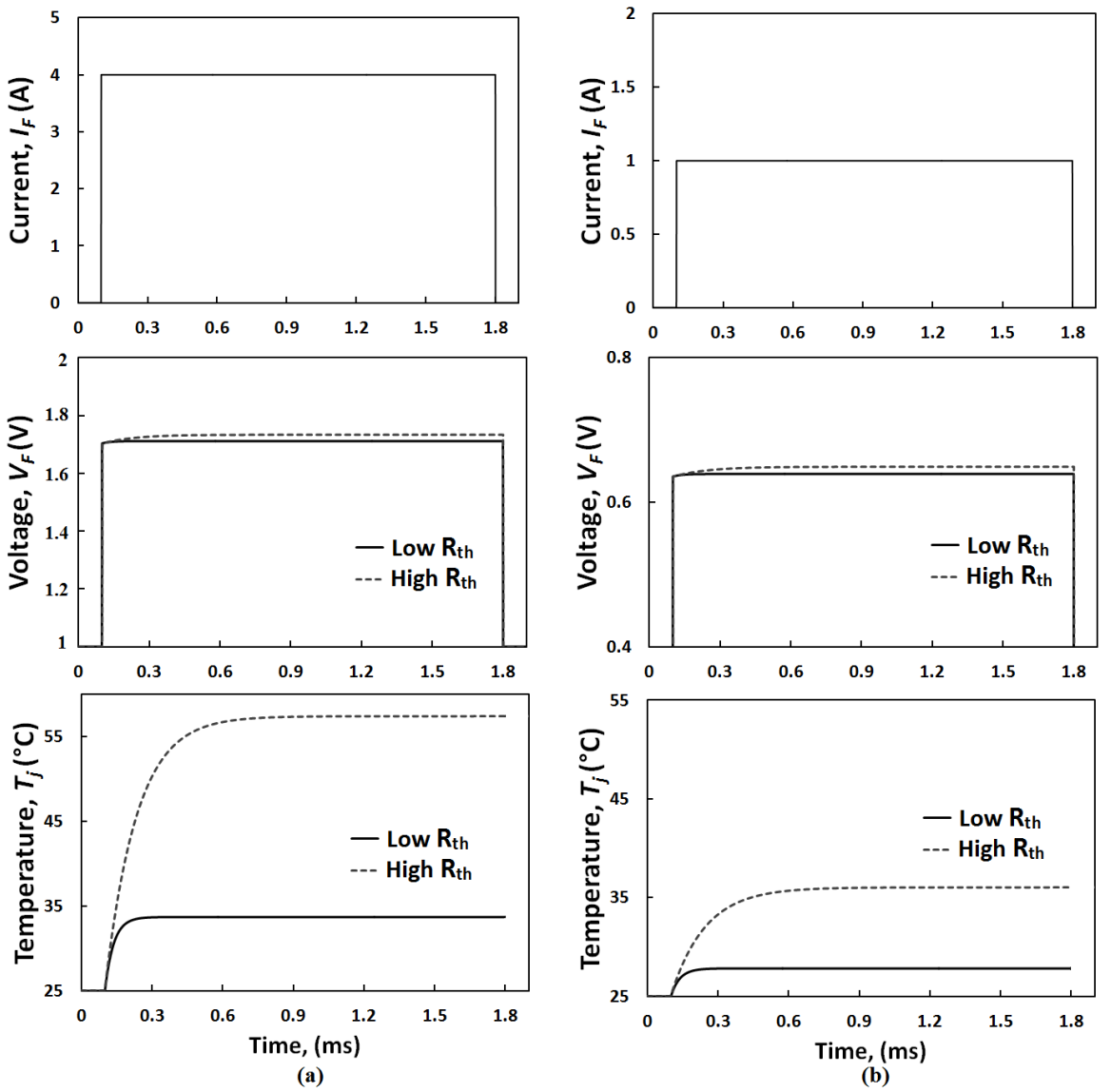

Fig. 3.8 Simulated I_F, V_F and Junction Temperature characteristics of the series connected SiC Schottky diodes for different current levels a) 4A b) 1A above the ZTC point.

3.2.3 Series Si IGBTs in ON-state

IGBTs are similar to thyristors in the sense that they are both 4-layer devices with 3 internal PN junctions. Hence, like thyristors, IGBTs are capable of bi-directional voltage blocking capability although punch-through and field-stop IGBTs are not. The primary difference between IGBTs and thyristors is that IGBTs are capable of self-turn-OFF and hence, do not rely on voltage reversal by the AC system. For this reason, IGBTs were implemented in voltage source converter topologies whereas thyristors are deployed in line commutated current source converter topologies. An n-channel IGBT can be thought of as a PNP BJT with a MOS gate. IGBTs can be non-punch-through (NPT) IGBTs or punch-through IGBTs (which later evolved into field-stop IGBTs) with the difference being the insertion of an N+ region between the P+ collector and the N- drift layer in the case of the field-stop (and punch-through) IGBTs. Fig.3.9 below shows a schematic of both IGBTs.

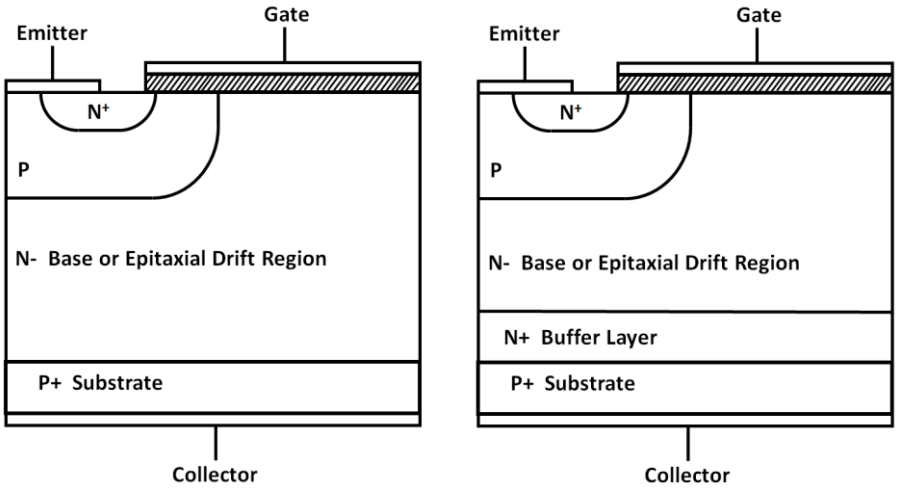

Fig. 3.9 NPT and PT IGBTs.

For high voltage applications, IGBTs generally perform better in the ON-state compared to unipolar devices like MOSFETs because of conductivity modulation which is enabled by electron-hole injection into the drift region of the IGBT. When in the ON-state, IGBT can be conceived of as a MOSFET in series with a PiN diode with the cathode connected to the source. Fig.3.10 shows 3 equivalent circuits of the IGBT with varying degrees of complexity. Fig.3.10 (a) shows the MOSFET in series with the PiN diode schematic, while Fig.3.10 (b) shows the MOS driven PNP BJT model and Fig.3.10 (c) includes the parasitic NPN BJT in the model shown in (b).

The forward voltage of the IGBT can be derived simply by adding the forward voltage of the MOSFET channel to that of the PiN diode as is done in equation 3.32 below [3,5].

$$V_{IGBT} = V_{ch} + V_{PiN} \tag{3.32}$$

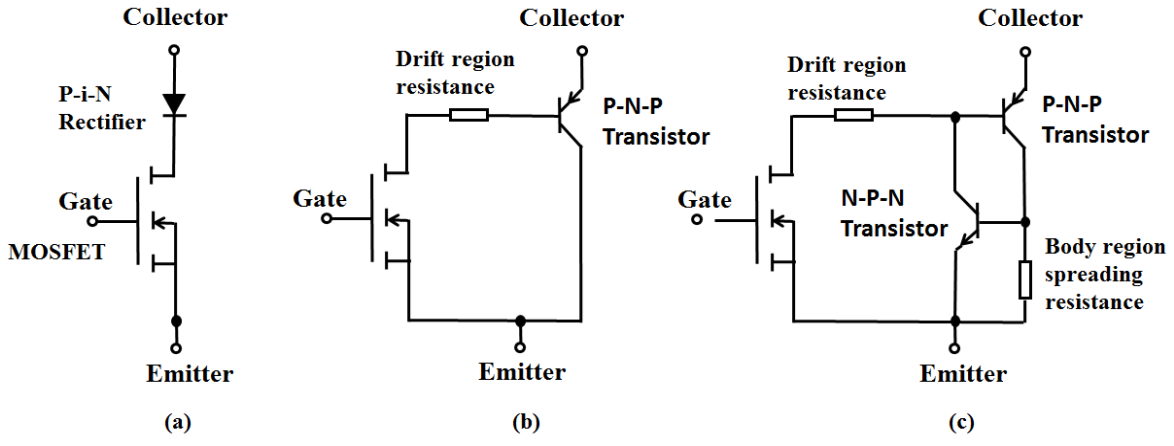

Fig. 3.10 Equivalent circuits of the IGBT (a) PiN diode model (b) MOS and PNP BJT model and (c) MOS and PNP BJT.

The forward voltage of the PiN diode is given by [3]:

$$V_{PiN} = \frac{2kT}{q}\ln\left(\frac{J_C W}{4qD_a n_i F(W/2L_a)}\right) \tag{3.33}$$

$F\left(\frac{W}{L_a}\right)$ is complex function. The on-state voltage drop is smaller if the function F is large. The variation of the function $F\left(\frac{W}{L_a}\right)$ with increasing $\left(\frac{W}{L_a}\right)$ ratio is fully described in [3]. The function has maximum value when $\frac{W}{L_a} = 1$. To reduce the on-state voltage drop, the lifetime needs to be corrected until the L_a is equal to $\frac{W}{2}$. It is worth to note the function reduces dramatically when the $\left(\frac{W}{L_a}\right)$ ratio increases beyond a value of 3.

Hence, the total forward voltage of the IGBT is given by:

$$V_{IGBT} = \frac{J_C LW}{2\mu C_{OX}(V_{GS} - V_{TH})} + \frac{2kT}{q}\ln\left(\frac{J_c W}{4qD_a n_i F(W/2L_a)}\right) \tag{3.34}$$

where D_a is the ambipolar diffusivity, L_a is the minority carrier diffusion length and $F(W/(2L_a))$ is a dimensionless variable that depends on the ratio between the hole diffusion length in the drift region and the thickness of the drift region in the IGBT. Compared to the equation for the forward voltage of the MOSFET, the 2nd component of equation 3.33 depends on the bipolar characteristics of the IGBT and not the drift layer blocking resistance. This is what makes IGBTs more suitable for high voltage applications than MOSFETs. The temperature dependency of the IGBTs forward voltage will be a combination both the MOS component and the bipolar component. As discussed previously, the MOS channel component exhibits a temperature dependency

that can be positive or negative depending on whether the effective mobility or the threshold voltage dominates. To determine the total temperature dependency of the IGBT forward voltage, the temperature dependency of the PiN diode forward voltage as well as that of the MOS channel must be taken into account.

The derivative of the PiN diode's forward voltage with respect to temperature is given by:

$$\frac{dV_{PiN}}{dT} = \frac{2k}{q}\left(\ln\left(\frac{J_F W_d}{4qD_a n_i F\left(\frac{W_d}{2L_a}\right)} \right) - \frac{T}{D_a n_i}\left(D_a \frac{dn_i}{dT} + n_i \frac{dD_a}{dT} \right) \right) \tag{3.35}$$

where the ambipolar diffusivity is given by [20]:

$$D_a = \frac{2kT}{q}\frac{\mu_n \mu_p}{\mu_n + \mu_p} \tag{3.36}$$

And its temperature derivative is given by:

$$\frac{dD_a}{dT} = \left(1.72\times10^{-4} \frac{\mu_n \mu_p}{\mu_n + \mu_p} \right) + \left(1.72\times10^{-4} \frac{T}{\left(\mu_n + \mu_p\right)^2} \right)\left(\frac{d\mu_n}{dT}\mu_p{}^2 + \frac{d\mu_p}{dT}\mu_n{}^2 \right) \tag{3.37}$$

The temperature derivatives of the electron and hole mobilities in Silicon, empirical relationships are given by:

$$\frac{d\mu_n}{dT} = -10.96\left(\frac{T}{300} \right)^{-3.42} \tag{3.38}$$

$$\frac{d\mu_p}{dT} = -3.63\left(\frac{T}{300}\right)^{-3.20} \tag{3.39}$$

In equation 3.34, it is assumed that the temperature dependency of the intrinsic carrier concentration dominates the temperature dependency of the $F(W/(2L_a))$ function. The $F(W/(2L_a))$ function is assumed to be temperature invariant since the temperature dependency of the ambipolar diffusion length (L_a) is significantly smaller than the temperature dependency of the intrinsic carrier concentration. The ambipolar diffusion length is given by [3,10]:

$$L_a = \sqrt{D_a \tau} \tag{3.40}$$

The ambipolar diffusivity (D_a) decreases with temperature according to equation 3.36 due to the decrease of the effective mobility while the carrier lifetime increases with temperature. The net effect causes a low temperature dependence L_a.

In the equation 3.34, the dominant temperature dependent parameter is the intrinsic carrier concentration which increases with temperature due to bandgap narrowing according to [3]:

$$n_i = \sqrt{N_C N_V}\, e^{\frac{E_G}{2kT}} \tag{3.41}$$

For Silicon,

$$n_i = 3.87 \times 10^{16} T^{1.5} e^{-\frac{7.02 \times 10^3}{T}} \tag{3.42}$$

$$\frac{dn_i}{dT} = \left(\frac{7.02 \times 10^3}{\sqrt{T}} + \frac{3\sqrt{T}}{2} \right) \left(3.87 \times 10^{16} \right) e^{-\frac{7.02 \times 10^3}{T}} \tag{3.43}$$

For SiC:

$$n_i = 1.70 \times 10^{16} T^{1.5} e^{-\frac{2.08 \times 10^4}{T}} \tag{3.44}$$

$$\frac{dn_i}{dT} = \left(\frac{2.08 \times 10^4}{\sqrt{T}} + \frac{3\sqrt{T}}{2} \right) \left(1.70 \times 10^{16} \right) e^{-\frac{2.08 \times 10^4}{T}} \tag{3.45}$$

The temperature dependence of the ON-state voltage of the IGBT will depend on the temperature coefficient of the PiN diode forward voltage as well as that of the MOS channel voltage drop. As has been shown previously, the ON-state voltage of the MOS channel will increase with temperature because of the reduced carrier mobility. However, the forward voltage of the PiN diode will decrease with temperature due to an increase in the intrinsic carrier concentration as shown in equations 3.42 for Silicon and 3.44 for SiC.

$$\frac{dV_{IGBT}}{dT} = \frac{dV_{ch}}{dT} + \frac{dV_{PiN}}{dT} \tag{l(3.46)}$$

Simulations of the temperature characteristics of silicon IGBTs have been performed in SILVACO [7] to investigate how the conflicting temeprature coefficients of the MOS channel and the IGBT impact the forward and transfer characteristics of the IGBT. Table 3.1 shows the simulation parameters used in the SILVACO model.

Table 3.1 IGBT simulation parameters and values

Parameter	Value
Source n doping (cm^{-3})	1×10^{19}
P body doping (cm^{-3})	5×10^{17}
Drift layer thickness (μm)	78
Drift layer doping (cm^{-3})	1×10^{14}
P+ collector doping (cm^{-3})	1×10^{19}
Gate Oxide thickness (nm)	80
Hole carrier lifetime (s)	1×10^{-7}

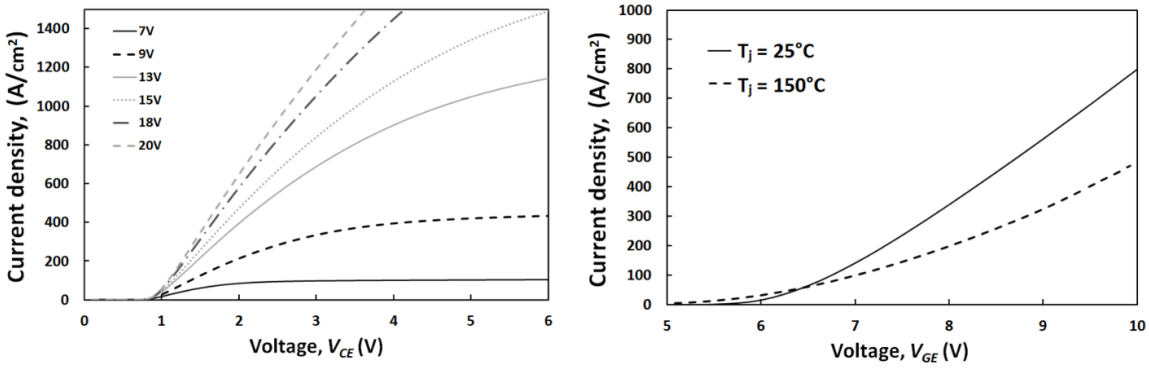

Fig. 3.11 Simulated I_{CE} vs V_{CE} characteristics of the silicon IGBT.

The results of the simulations are shown in Fig.3.11 which shows the gate transfer characteristics (I_{GE} vs V_{GE}) and the output characteristics (I_{GE} vs V_{CE}) at 2 different temperatures. As can be seen from both the gate transfer and output characteristics, at low current levels, the forward voltage reduces with temperature for a given current. Hence, the power dissipated by the IGBT, which is calculated as $V_{CE}I_{CE}$, reduces with

increasing temperature, which is never the case for MOSFETs when operated at the rated gate voltage.

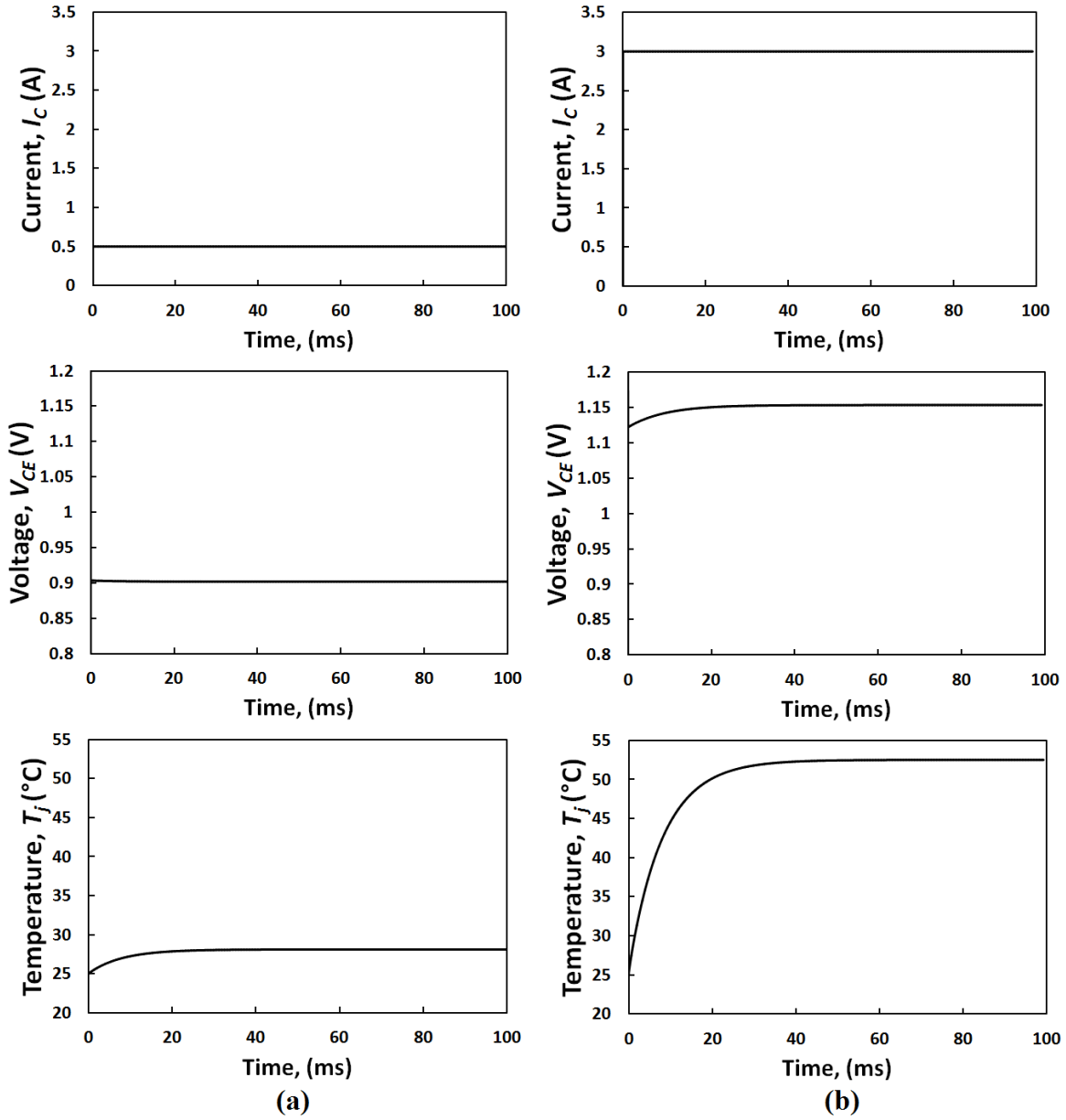

Fig. 3.12 Simulated I_{CE}, V_{CE} and Junction Temperature characteristics of the silicon IGBT for current levels below and above the ZTC point.

In applications where the IGBT is used with a large duty ratio and conduction losses dominate the total losses, the value of the load current will determine the thermal characteristics of the power device. Fig.3.12 (a) shows a simulated IGBT ON-state voltage and temperature as functions of time for the same IGBT conducting 50 A/cm^2 of current while Fig.3.12 (b) shows the same characteristics when the IGBT is conducting 150 A/cm^2. In Fig.3.12 (a), the current is below the ZTC point while in Fig.3.12 (b), the current is above the ZTC. It can be seen from Fig.3.12 (a), that when the load current is below the ZTC, the forward voltage decreases with time due to increased lattice heating. This means that the IGBT dissipates less power as the device gets hotter. On the other hand, if the load current is above the ZTC, as can be seen from Fig.3.12 (b), the forward voltage increases over time. This increases the power dissipated and the junction temperature until it reaches steady state when the rate of heat generation becomes equal to the rate of heat extraction.

Fig.3.13 (a) and (b) shows the simulated characteristics of the series connected Si IGBTs for current levels below and above ZTC point respectively.

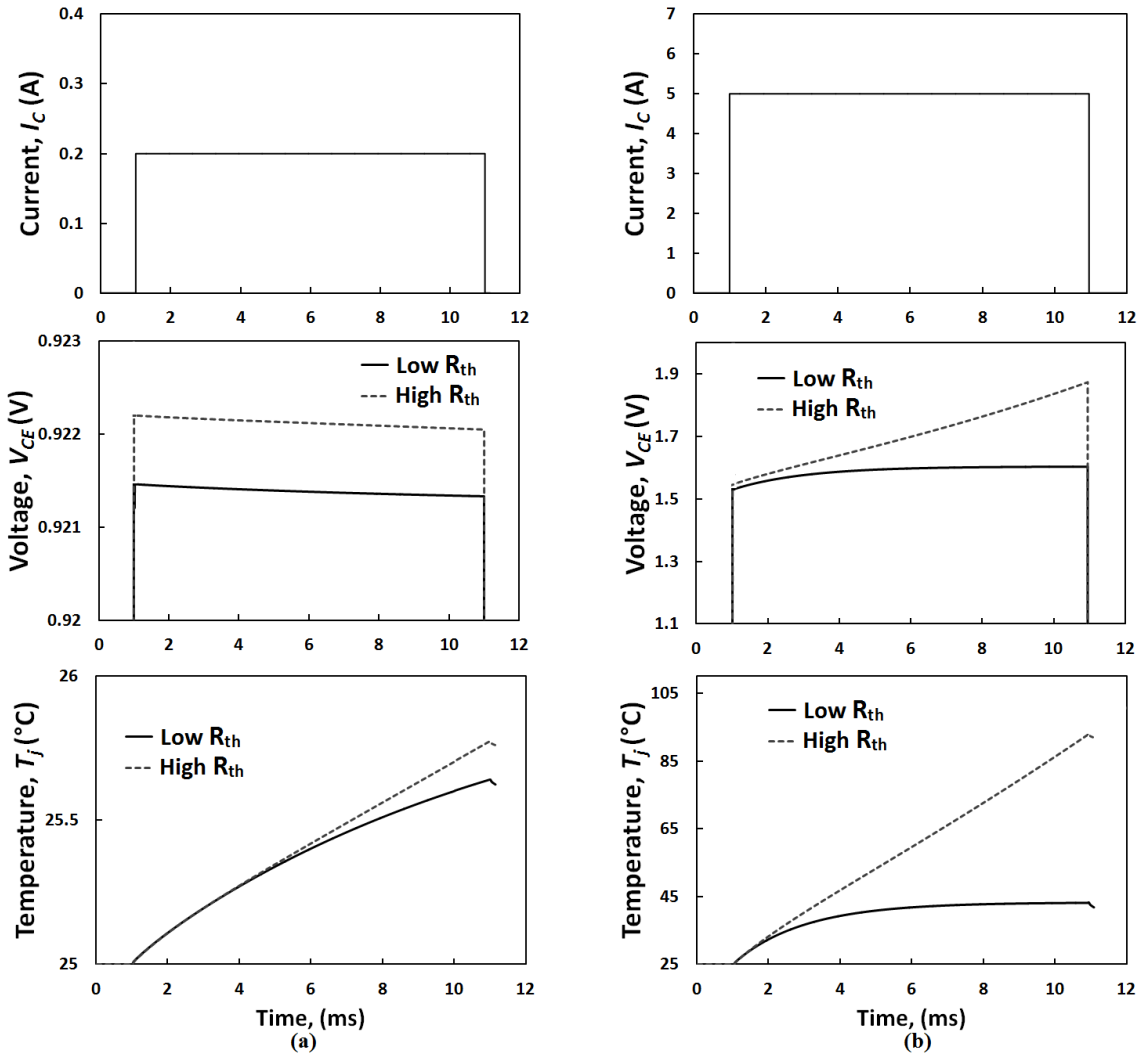

Fig. 3.13 Simulated I_{CE}, V_{CE} and Junction Temperature characteristics of the series connected Si IGBTs for current levels (a) below and (b) above the ZTC point

3.2.4 Series Silicon PiN diodes in the ON-state

The current at the ZTC point can be determined by setting the derivative in equation 3.34 to zero and solving for the forward current density. The current density at ZTC is given by [3, 21-22]

$$J_F = \frac{2qD_a n_i F\left(\frac{W_d}{L_a}\right)}{W_d} e^{\left(\frac{T}{D_a n_i}\left(D_a \frac{dn_i}{dT} + n_i \frac{dD_a}{dT}\right)\right)} \tag{3.46}$$

The ZTC current for a silicon PiN diode assuming 117 μm drift layer thickness, 600 V voltage rating, 16 mm² active area and $F(W_d/L_a)$=2.4 has been calculated as 16 A. Using the equations presented above, the forward voltage has been calculated as a function of temperature for different forward currents an plotted in Fig.3.14 shows the temperature dependency of the hypothetical PiN diode at three currents, one below the ZTC where the forward voltage has a negative temperature coefficient, one at the ZTC point where the forward voltage is temperature invariant and one above the ZTC where the forward voltage as a positive temperature coefficient.

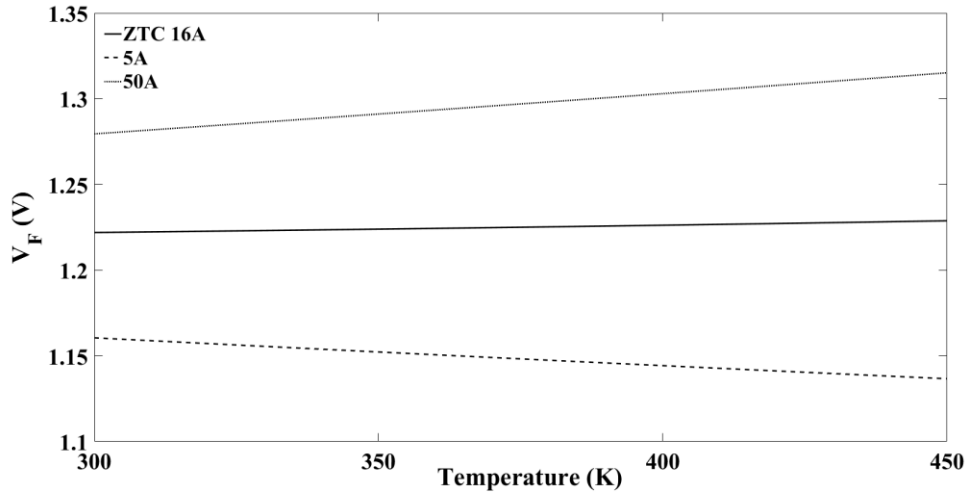

Fig. 3.14 The forward voltage as a function of temperature for different forward currents.

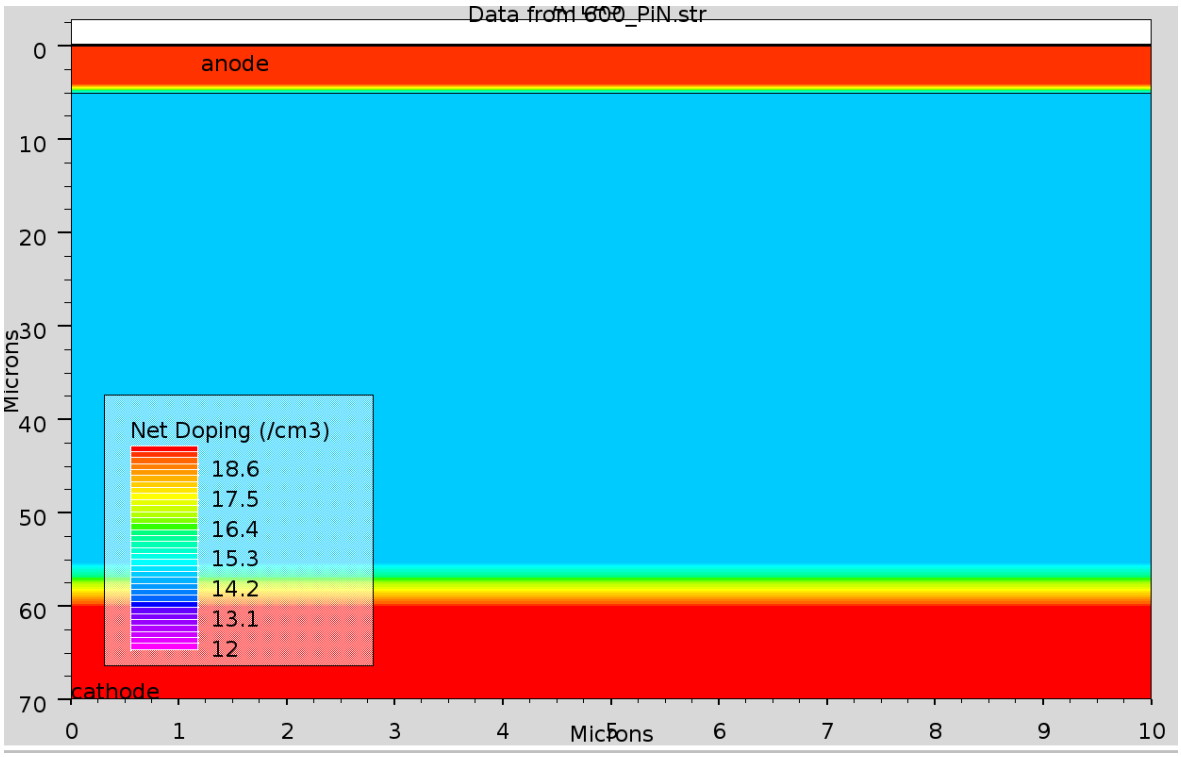

Fig. 3.15 The Si PiN diode model rated at 600V.

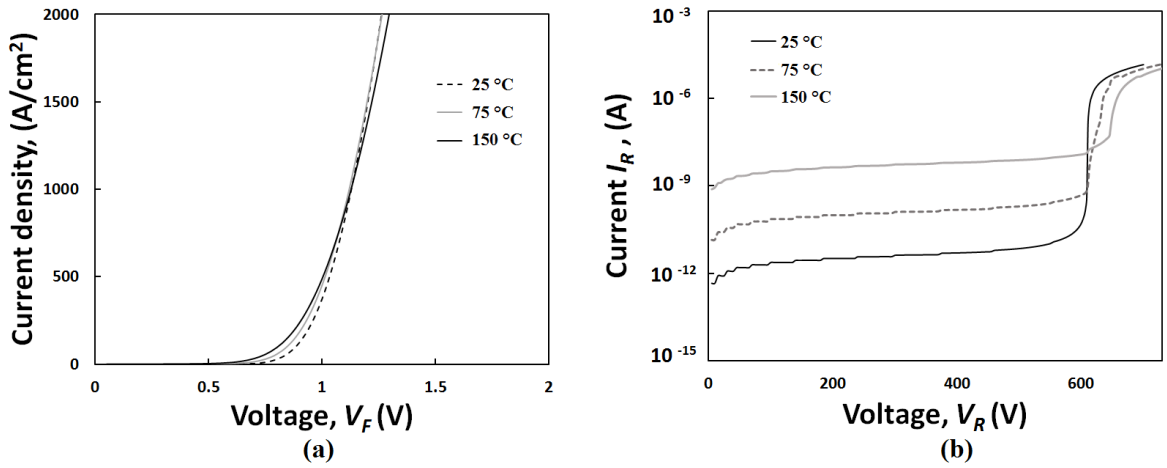

Fig. 3.16 Simulated forward and reverse characteristics of Si PiN diode.

Fig.3.15 shows an example of a finite element simulated 600V Si PiN diode with a drift layer thickness of 60μm and n-type doping level of 1×10^{15} cm^{-3}. Fig.3.16 shows the simulated forward and reverse characteristics of the Si PiN diode.

Fig.3.17 (a) and (b) shows the simulated characteristics of the series connected Si PiN diodes for different current levels for current of 4A and 1A above ZTC point respectively.

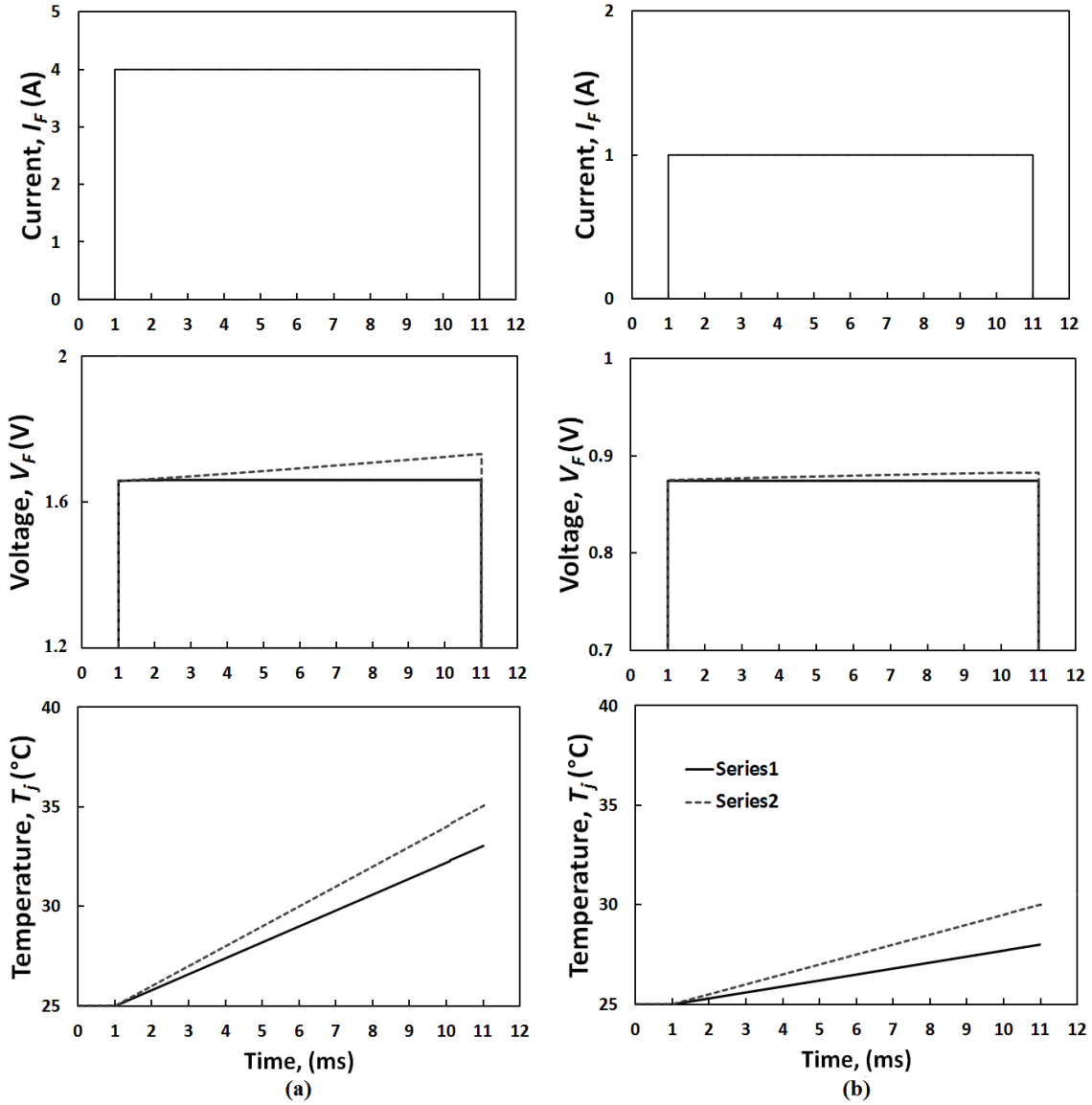

Fig. 3.17 Simulated I_F, V_F and Junction Temperature characteristics of the series connected Si PiN diodes for different current levels a) 4A b) 1A above the ZTC point.

3.2.5 Series Silicon IGBTs in OFF-state

When the IGBT is in the OFF-state and blocking voltage, the only current that flows through the collector is due to carrier generation in the depletion region. The depletion

region is formed mainly in the N-drift region of the IGBT as shown in Fig.3.18 for both the NPT and Field-stop IGBTs. As can be seen, the electric field profile in the NPT IGBT is triangular whereas that in the field-stop IGBT is trapezoidal.

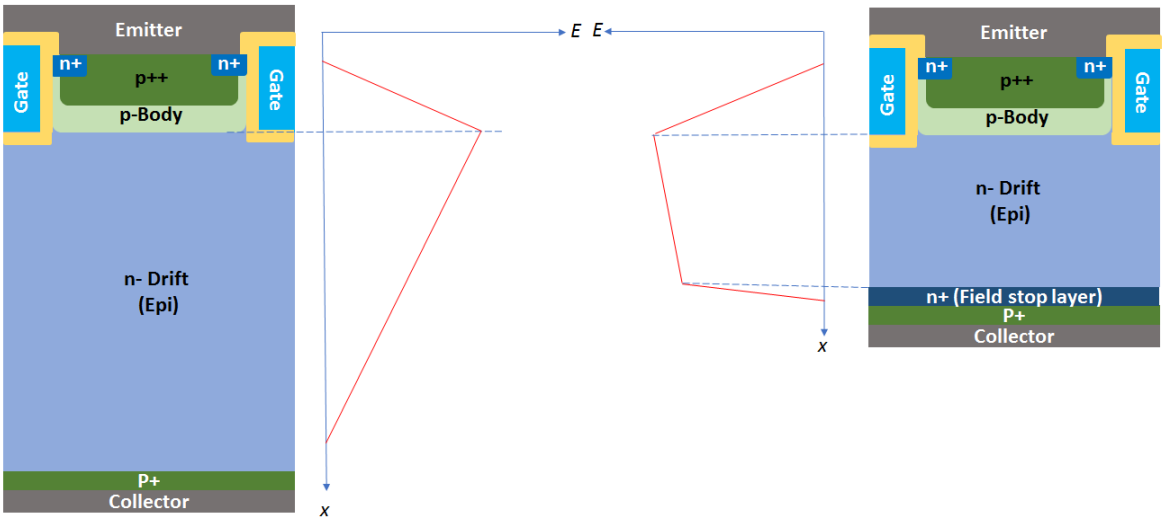

Fig. 3.18 Electric field profiles in NPT and Field-stop IGBTs.

The rate of carrier generation in the depletion region is determined by the space charge generation lifetime (the lifetime of a carrier before recombination). The high electric field causes some impact ionisation and the resulting drift velocity of the free carriers forms the leakage current which can be written as [3, 23-24]:

$$J_{SC} = \frac{qW_D n_i}{\tau_{SC}} \tag{3.47}$$

The depletion width under voltage blocking conditions can be derived from Gauss law by first applying it to the region of the IGBT depleting under the voltage

$$\int E.dA = \frac{Q}{\varepsilon_0 \varepsilon_r} \tag{3.48}$$

Considering that the total charge Q is equal to the number of depleted donor atoms (N_D) per cubic centimeter multiplied by the volume (Ax) being depleted:

$$EA = \frac{qN_A Ax}{\varepsilon_0 \varepsilon_r} \tag{3.49}$$

Since the electric field is the derivative of the collector voltage (V_{CE}) with distance:

$$\frac{dV_{CE}}{dx} = \frac{qN_A x}{\varepsilon_0 \varepsilon_r} \tag{3.50}$$

Hence, the collector voltage can be derived as:

$$V_{CE} = \frac{qN_A W_D^2}{2\varepsilon_0 \varepsilon_r} \tag{3.51}$$

The depletion width can be related to the collector voltage:

$$W_D = \sqrt{\frac{2\varepsilon_0 \varepsilon_r V_{CE}}{qN_D}} \tag{3.52}$$

Substituting equation (3.51) into equation (3.52) can yield a new expression for the space charge generation current:

$$I_{SC} = \frac{An_i}{\tau_{SC}} \sqrt{\frac{2q\varepsilon_0 \varepsilon_r V_{CE}}{N_D}} \tag{3.53}$$

The final expression for the IGBT leakage current can be derived simply by considering the contribution of both the space charge generation current and the hole current caused by carriers injected across the forward biased p+ collector junction. Fig. 3.19 shows a cross-section of an NPT IGBT under forward blocking condition where junction J_1 (the collector/drift P+/N junction) is forward biased and junction J_2 (p-body to N-drift junction) is reverse biased. Also shows the electric field profile under normal conditions and under reach-through (when the depletion width extends across the entire N drift region) conditions [3].

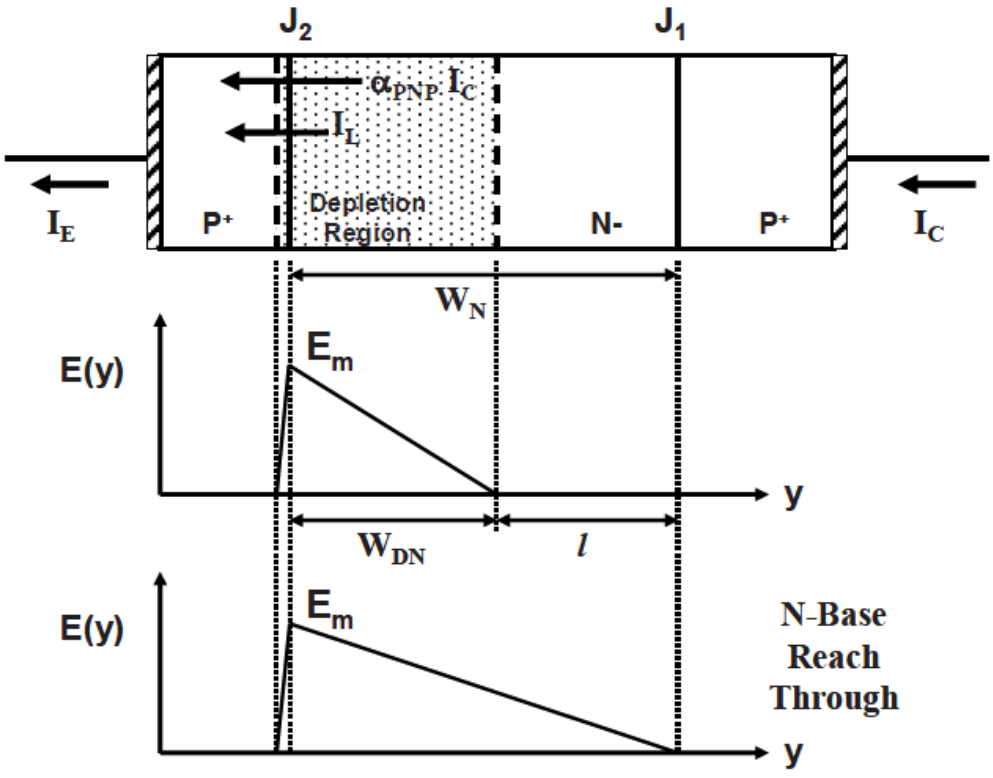

Fig. 3.19 IGBT under forward blocking conditions [3].

The hole current (caused by hole injection across the forward biased collector junction) flows across the PNP BJT which is in open base configuration, hence, is multiplied by the open base gain of the BJT. Hence, the total leakage current of the IGBT is the sum of the space charge generation current derived earlier and the collector current multiplied by the gain of the BJT [3,22].

$$I_{leak} = \alpha_{PNP} I_{leak} + I_{SC} \tag{3.54}$$

The final expression for the leakage current is:

$$I_{SC} = \frac{An_i}{\tau_{SC}(1-\alpha_{PNP})} \sqrt{\frac{2q\varepsilon_0\varepsilon_r V_{CE}}{N_D}} \tag{3.55}$$

When IGBTs are connected in series in the OFF-state, the leakage current flowing through the series connection will determine the sharing of the OFF-state voltage. It is useful to express the OFF-state blocking voltage in terms of the OFF-state current.

$$V_{CE} = \frac{N_D}{2q\varepsilon_0\varepsilon_r} \left(\frac{\tau_{SC}(1-\alpha_{PNP}) I_{SC}}{An_i} \right)^2 \tag{3.56}$$

3.3 Experimental Measurements of Series Devices in ON-state

Measurements in series connected power devices have been performed using the test-rig shown in Fig. 3.20. The test-rig set up includes: (1) Current Supply. (2) Voltage Supply. (3) Voltage probes. (4) DUTs. (5) Gate Drives. The devices under investigation are 600 V/20A Infineon Field Stop IGBTs with datasheet reference IKW20N60H3, 650 V/39A ROHM Trench SiC power MOSFET with datasheet reference SCT3060AL, 1.2kV/5A Wolfspeed SiC Schottky diode with datasheet reference C4D02120A and 1.2kV/8A Fairchild Si PiN diode with datasheet reference RHRP8120.

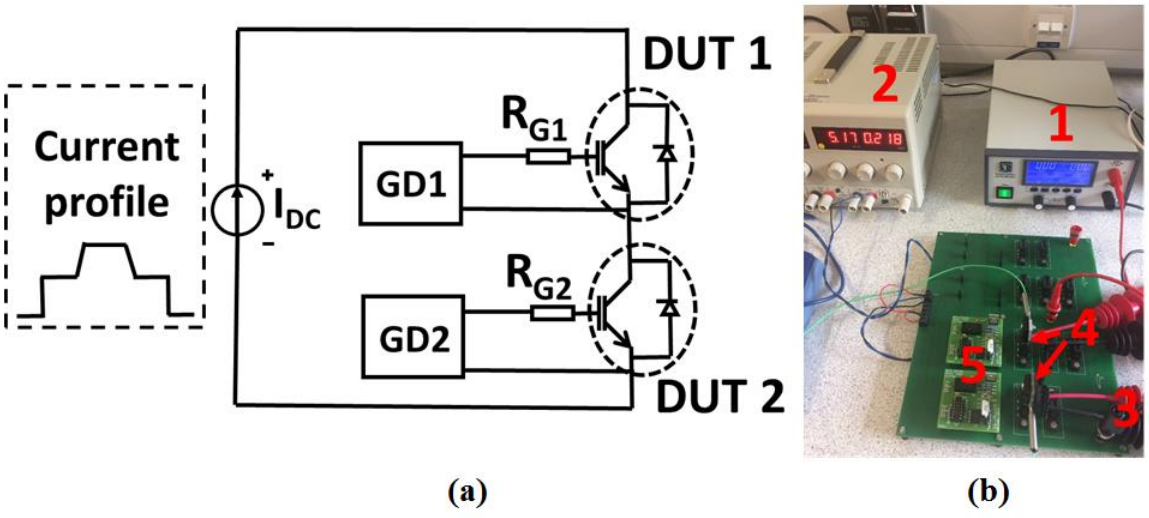

Fig. 3.20 (a) Circuit schematic and (b) test rig setup.

During the experiments, two power devices were connected in series and a trapezoidal current was passed through them for duration of about 150 seconds using a current

source. The voltage across each device was measured on an oscilloscope. Thermal variation between the devices was introduced by varying the sizes of the heatsink connected to both devices. This way, both devices were self-heated through conduction losses, however, the device with the smaller heatsink would exhibit higher junction/case temperatures. By varying the current level fed to the series connected devices, the voltage sharing between the devices below and above ZTC was investigated. The circuit schematic and test-rig is shown in Fig. 3.20.

Electro-thermal variation is introduced between the series connected devices by using different size heat-sinks. This is valid as the unbalanced electro-thermal degradation due to unbalanced voltage sharing leads to different junction temperatures between the two devices. The DUT with the smaller heatsink will therefore have a higher thermal resistance and a higher case temperature. During the experiment, the devices were thermally isolated. This was deliberately introduced to decouple the impact of the lateral heat transfer and emphasize only on the voltage unbalanced purely caused by the device degradation. For the experiments, a load current mission profile was programmed into the devices. The trapezoidal current profile used in the experiment is selected to investigate the impact of operation below and above the ZTC point on the voltage sharing during the ON-state operation. The trapezoidal current is shown in Fig. 3.22.

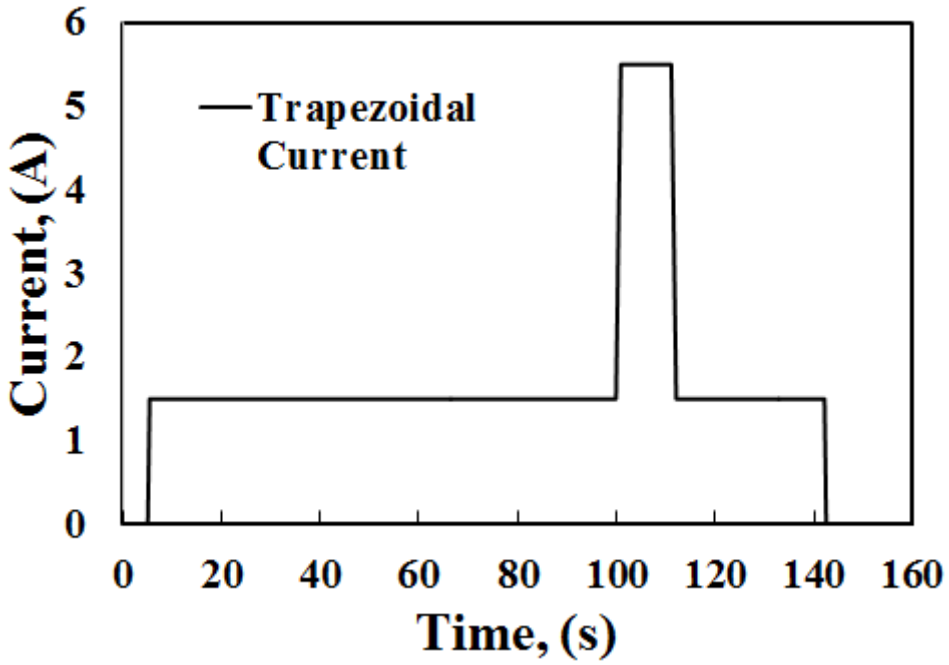

Fig. 3.21 Trapezoidal current.

Under normal operation of an inverter, the current waveform is usually sinusoidal which is achieved by applying a PWM signal to the gates of the switches. The switches carry a certain DC current during each ON-state period which can be either below or above the ZTC point. Hence, the voltage sharing between the series connected devices can vary based on the DC value of current. The forward voltage and corresponding case temperature were monitored for both devices. Fig.3.22 shows the ON-state voltage sharing between the two series connected Si IGBT and its corresponding temperature rise. The ON-state voltage sharing and its corresponding temperature of SiC MOSFET is presented in Fig.3.23. When the current is below the ZTC point in IGBTs, the hotter

device has a lower V_{ce} and when the device is operating above the ZTC, this is inversed. This was not evident in case of SiC MOSFET due to the very low ZTC of this device.

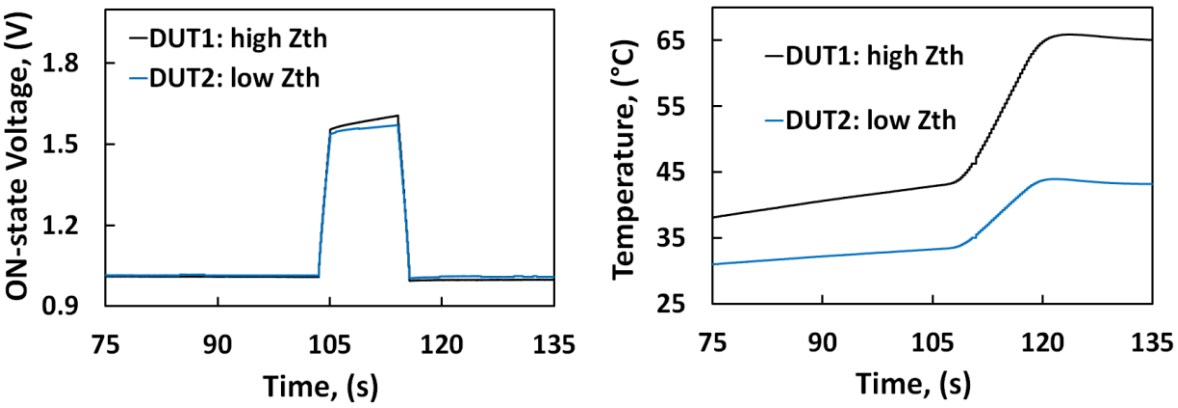

Fig. 3.22 Experimental results of ON-state voltage sharing above/below ZTC and case temperature of series connected Si IGBTs.

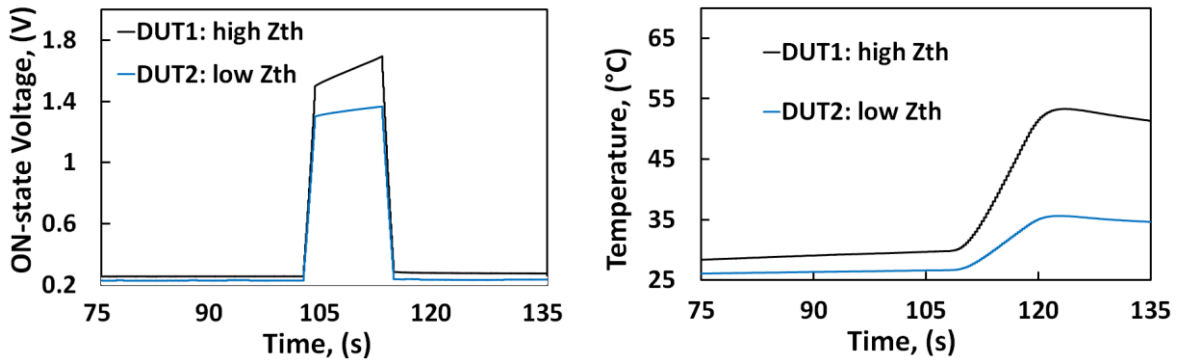

Fig. 3.23 Experimental results of ON-state voltage sharing and case temperature of series connected SiC MOSFETs.

The same measurements have been done for Si PiN diodes and SiC Schottky diodes results as shown in Fig.3.24 and Fig.3.25 respectively.

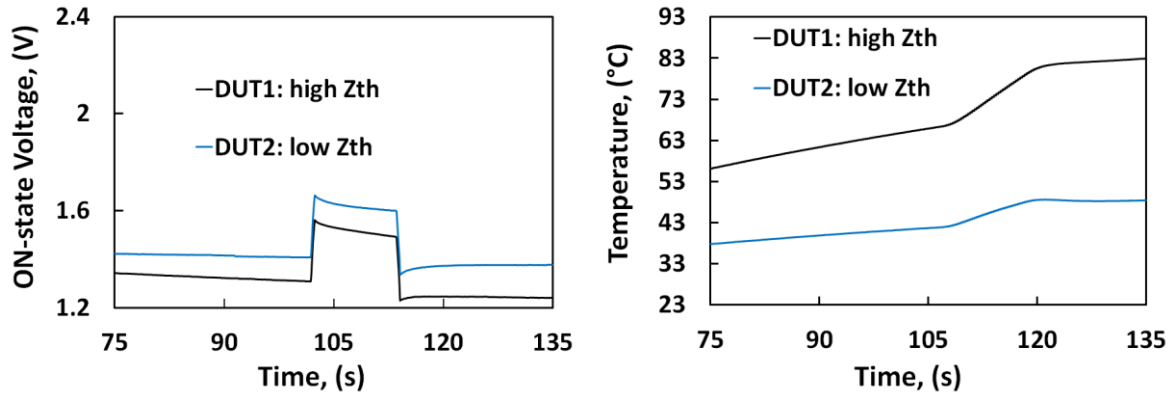

Fig. 3.24 Experimental results of ON-state voltage sharing and case temperature of series connected PiN diodes.

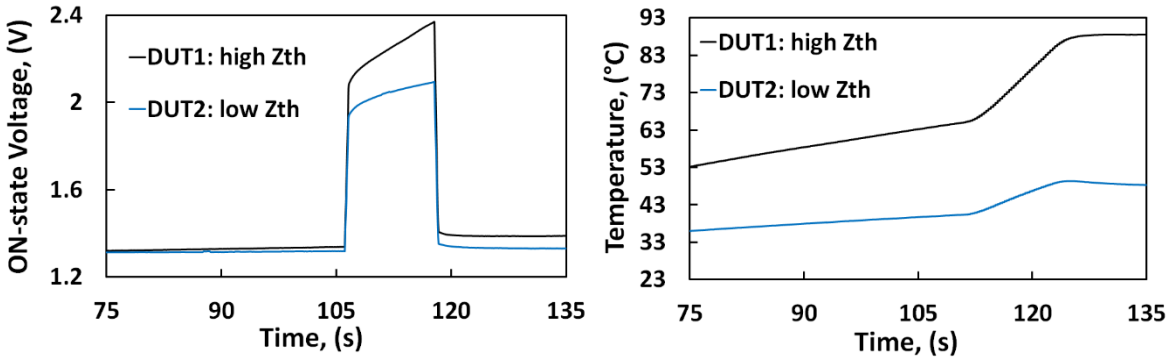

Fig. 3.25 Experimental results of ON-state voltage sharing and case temperature of series connected SiC Schottky diodes.

3.4 Model Development

A compact electrothermal model of two series connected power devices was developed in Matlab/Simulink. The model consists of 2 series connected devices with variable junction to case thermal impedances (Z_{th}). Fig. 3. shows a block diagram of the electrothermal model. The model comprises of a current source which supplies a load current mission profile. The temperature-dependent forward characteristics of the

devices were obtained from static temperature measurements and validated against the datasheets provided by the device manufacturers. Next, the conduction power losses of the two series devices were fed to the Cauer-thermal network of each of the devices. The junction temperature obtained from the Cauer-thermal network was used as a feedback to the temperature dependent forward characteristic lookup table to obtain the correct temperature dependent on-state losses for the next time step of the simulation.

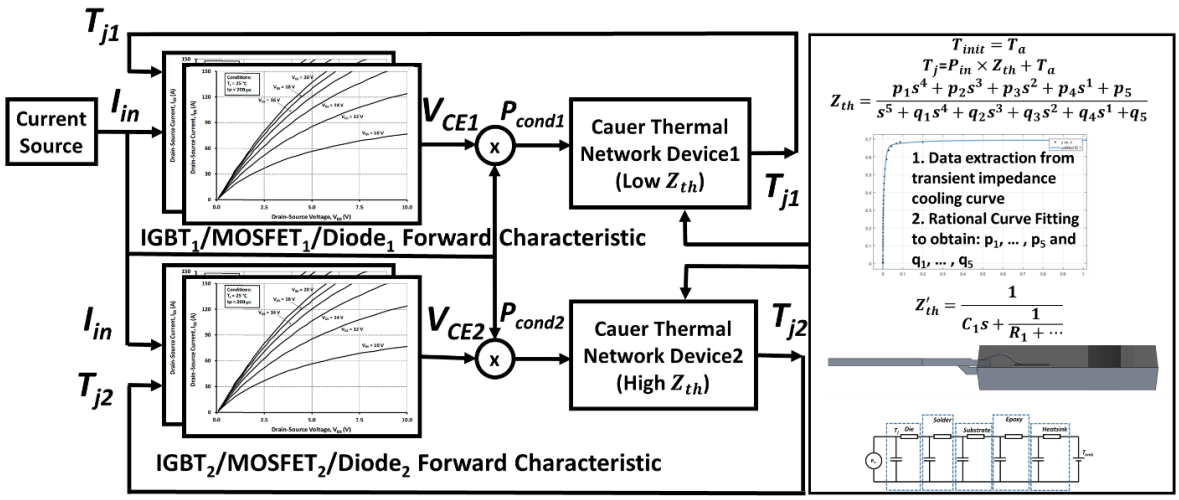

Fig. 3.26 Block diagram of electro-thermal model.

In order to obtain the Cauer-thermal network parameters, the transient thermal impedance of the TO-247 (for transistors) and TO-220 (for diodes) packages of devices were obtained through the datasheet and a finite number of elements were chosen and extracted on the curve. A rational curve fitting tool was used with specified lower and upper boundaries for each of the Cauer-thermal network parameters based on the device geometry to obtain the coefficients of the rational equation shown on the right-

hand box of Fig.3.26. In the next step, the transpose of the rational curve fitting equation was used to calculate the thermal resistance and thermal capacitances of each layer of Cauer-thermal network. The values were validated through experimental results to have a match between the case temperature of the devices when a trapezoidal current with a certain duration was applied to the device and the case temperature was measured using a thermocouple attached to the back plate of the device. A resistor in series with a voltage source denoting the heat convection coefficient through air and the room temperature respectively were used at the last Cauer-thermal network layer. The value of heat transfer coefficient was obtained from the heatsink datasheet of the device.

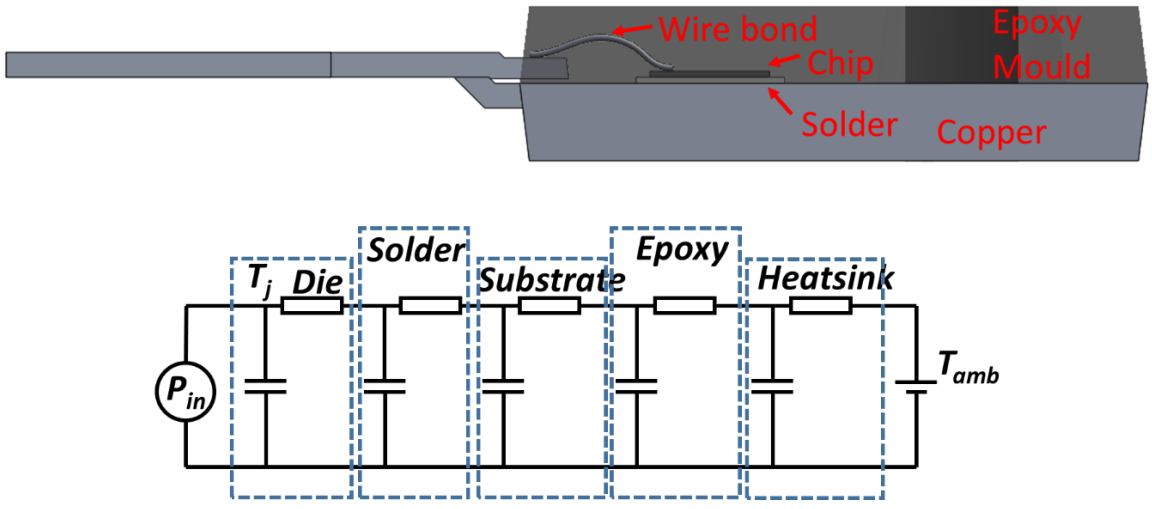

Fig. 3.27 Cross-section view of the package of discrete device and the corresponding Cauer-network of the device.

Fig.3.28 illustrates all layers considered in TO-247 package and its corresponding Cauer thermal network. The Cauer thermal network is comprised of 5 layers: die, solder attach, standard copper base metal, CTE-matched epoxy and moulding compound encapsulation.

In [11], details the method of extracting the coefficients of the transfer function. The reconstruction of the thermal impedance using rational curve is given by equation (3.57).

$$Z_{th} = \frac{p_1 s^4 + p_2 s^3 + p_3 s^2 + p_4 s + p_5}{s^5 + q_1 s^4 + q_2 s^3 + q_2 s^4 + q_1 s^1 + q_5} \tag{3.57}$$

In this equation, 5 layers of Cauer-thermal network determines the denominator degree in the rational polynomial equation. The impedance from the junction to case is reconstructed and calculated using equation (3.58):

$$Z_{th} = \cfrac{1}{C_1 s + \cfrac{1}{R_1 + \cfrac{1}{\ldots + \cfrac{1}{C_i s + \cfrac{1}{R_i}}}}} \tag{3.58}$$

As mentioned earlier, the values of thermal resistances and capacitances have been restricted within limits based on the device geometry and physical constants. A good fit between the datasheet thermal impedance curve and the fitted curve is provided based on the method explained. Fig.3.28 shows the comparison between the extracted points of the transient thermal impedance of a SiC MOSFET obtained from the

manufacturer's datasheet and the fitted curve based on the rational polynomial equation explained above. As can be seen, there is a good alignment between the fitted curve and the extracted curve.

Table 3.2 Thermal resistance and thermal capacitance for devices calculated from the transient thermal impedance curve of devices

Thermal parameters	Si PiN diode	SiC Schottky diode	Si IGBT	SiC MOSFET
R_1 [K/W]	0.0101	0.3204	0.08715	0.17998
R_2 [K/W]	0.1832	0.153	0.2547	0.08094
R_3 [K/W]	0.2853	0.469	0.35	0.2618
R_4 [K/W]	0.1655	0.08042	0.09332	0.2845
R_5 [K/W]	0.01198	0.1151	0.02523	0.2137
C_1 [J/K]	0.0249	2.847×10^{-4}	1.012×10^{-4}	3.387×10^{-4}
C_2 [J/K]	6.07×10^{-4}	1.456×10^{-3}	1.956×10^{-3}	1.174×10^{-3}
C_3 [J/K]	0.01036	3.338×10^{-2}	3.327×10^{-2}	6.889×10^{-4}
C_4 [J/K]	0.1655	0.4557	0.6798	5.318×10^{-4}
C_5 [J/K]	0.01198	0.4402	0.6176	0.0587

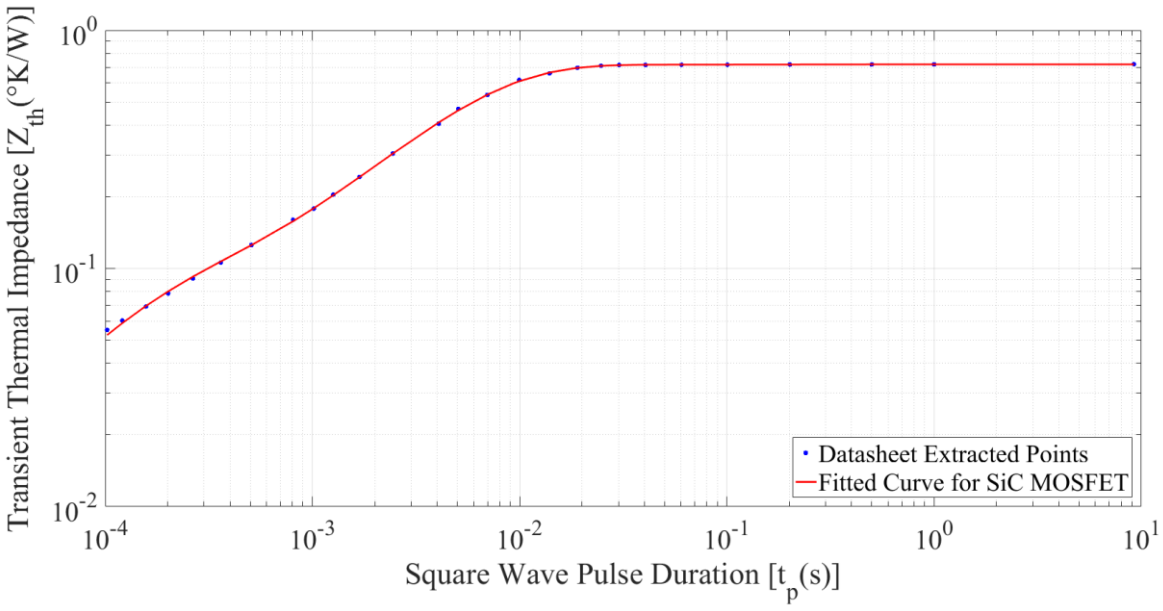

Fig. 3.28 Fitted curve of the transient thermal impedance of SiC MOSFET.

Similarly, Fig.3.29 - Fig.3.31 show the comparison between the transient thermal impedance of the Si IGBT, Si PiN diode and SiC Schottky diode respectively which were used in experiments in this chapter.

The goodness of the fit for the SiC MOSFET thermal transient curve is:

Goodness of fit:

SSE: 0.0001858

R-square: 0.9999

Adjusted R-square: 0.9999

RMSE: 0.003306

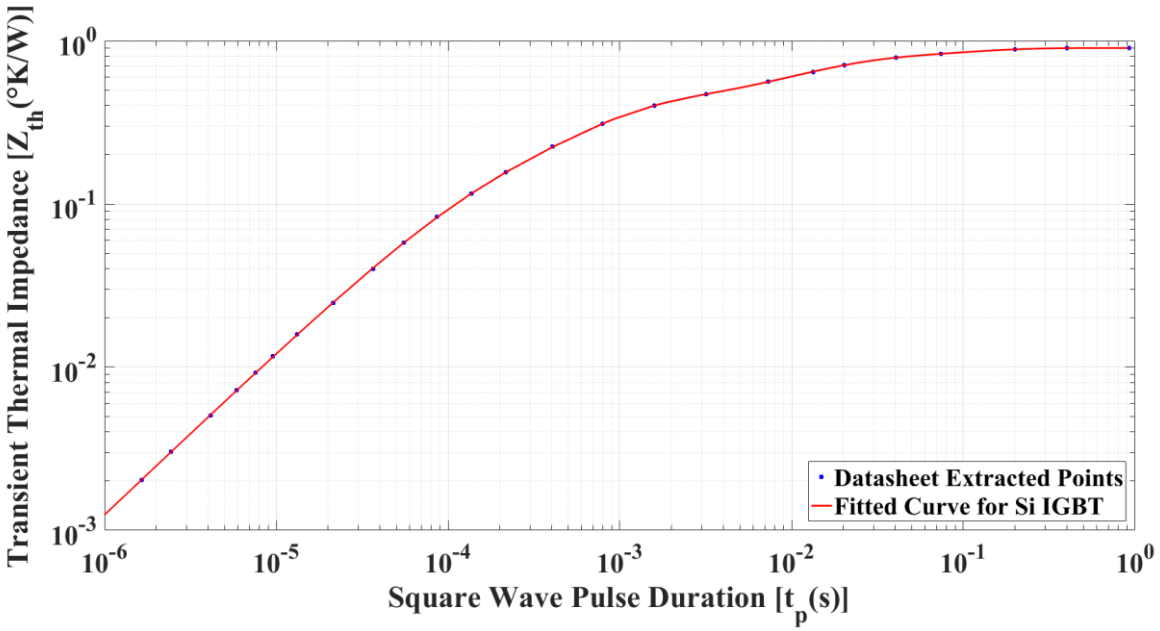

Fig. 3.29 Fitted curve of the transient thermal impedance of Si IGBT.

The goodness of the fit for the Si IGBT thermal transient curve is:

Goodness of fit:

SSE: 1.643e-05

R-square: 1

Adjusted R-square: 1

RMSE: 0.001013

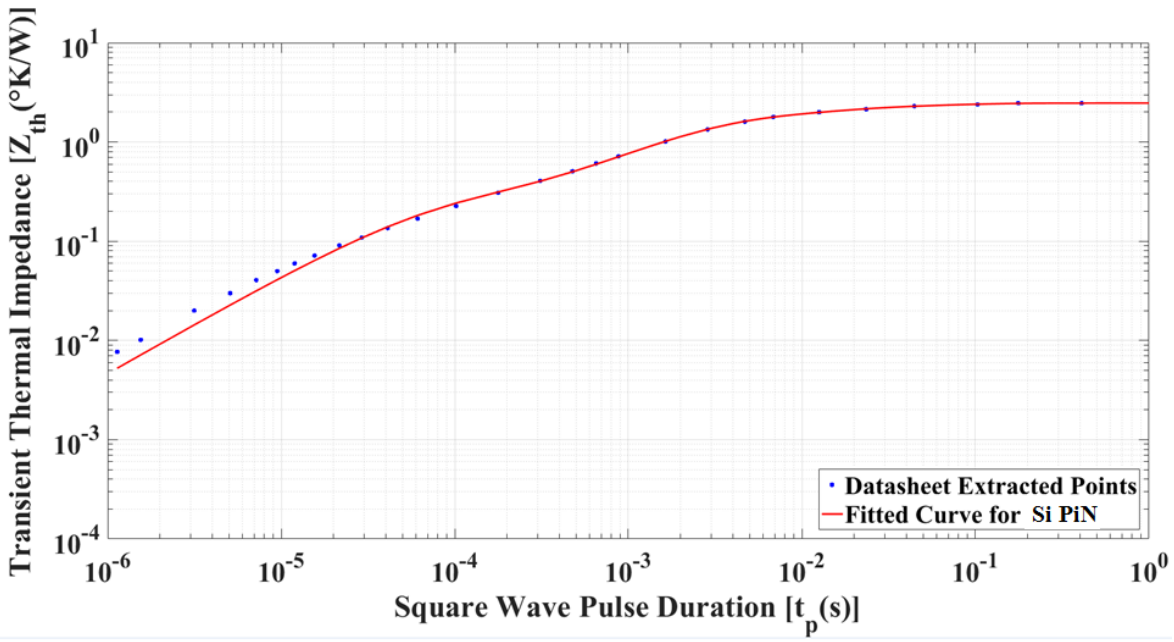

Fig. 3.30 Fitted curve of the transient thermal impedance of PiN diode.

The goodness of the fit for Si PiN diode thermal transient curve is:

Goodness of fit:

SSE: 0.002476

R-square: 0.9999

Adjusted R-square: 0.9999

RMSE: 0.01207

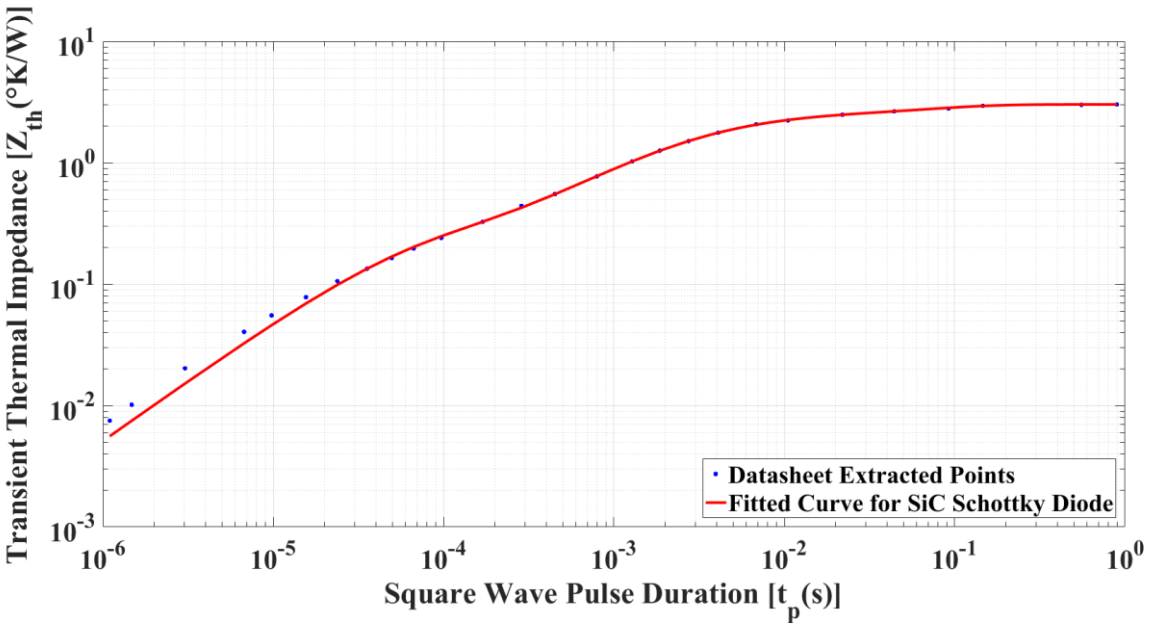

Fig. 3.31 Fitted curve of the transient thermal impedance of SiC Schottky Diode.

The goodness of the fit for SiC Schottky diode thermal transient curve is:

Goodness of fit:

SSE: 0.003544

R-square: 0.9999

Adjusted R-square: 0.9998

RMSE: 0.01403

The simulation results of ON-state voltage sharing above/below ZTC and case temperature of series connected power devices: Si IGBTs, SiC MOSFETs, PiN diodes and Schottky diodes are shown in Fig.3.32 – Fig.3.35 accordingly. As explained earlier,

the temperature dependent forward characteristic of the devices used in the simulation were obtained from the device datasheet and using the extracted Cauer-thermal network explained earlier, the junction temperature of the devices under different forward currents (below and above ZTC point) were modelled. As can be seen, the simulated results show a very good correlation between the experimental results.

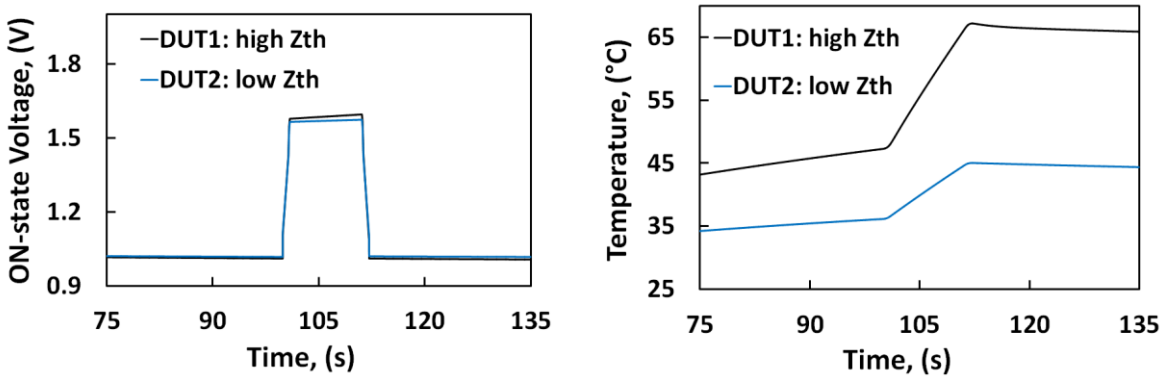

Fig. 3.32 Model-based simulation results of ON-state voltage sharing above/below ZTC and case temperature of series connected Si IGBTs.

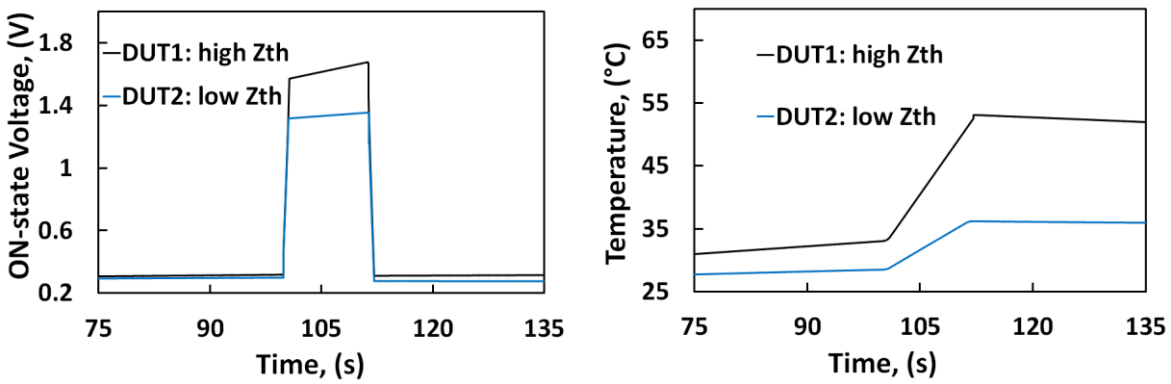

Fig. 3.33 Model-based simulation results of ON-state voltage sharing and case temperature of series connected SiC Trench MOSFETs.

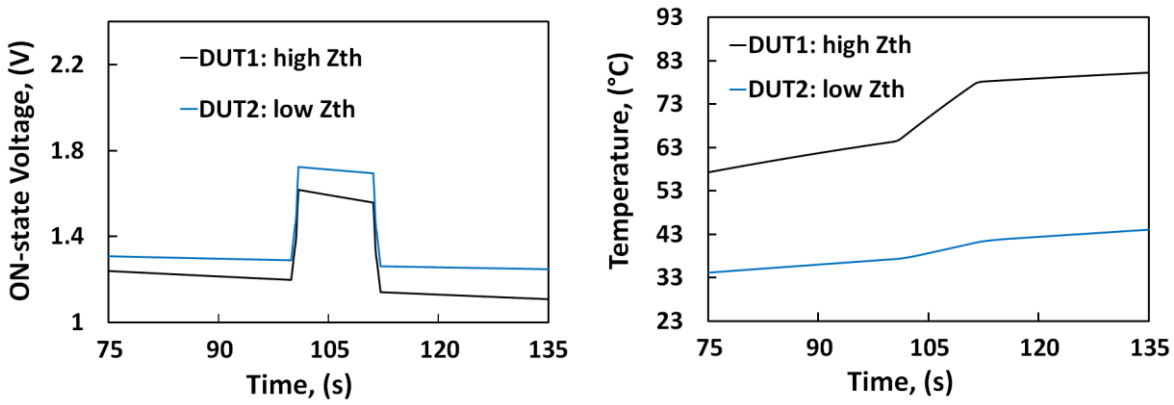

Fig. 3.34 Model-based simulation results of ON-state voltage sharing and case temperature of series connected Si PiN diodes.

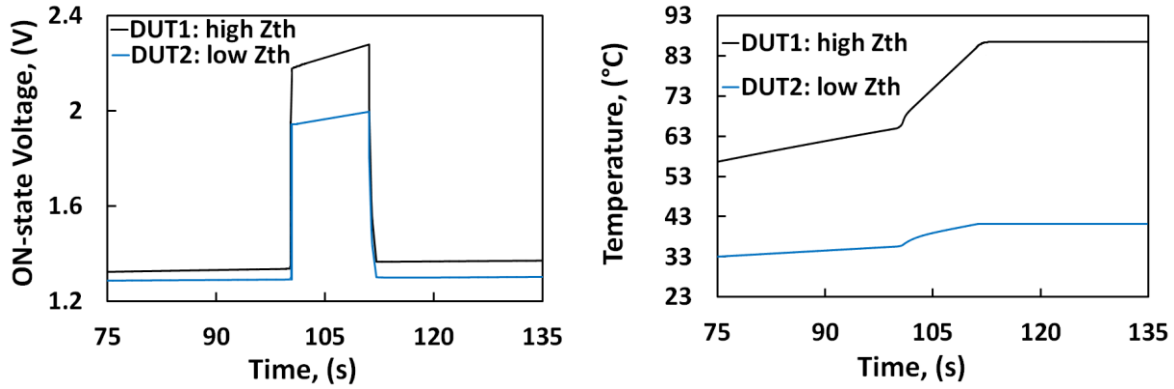

Fig. 3.35 Model-based simulation results of ON-state voltage sharing and case temperature of series connected SiC Schottky diodes.

3.5 OFF-State Voltage Sharing

The differences in electrothermal properties of devices may cause variation in the OFF-state voltage blocking capability of the series connected devices. The physical architecture of cooling systems in series connected power devices may cause some inevitable temperature variation between series connected power modules, hence, differences in temperature induced leakage current may cause OFF-state voltage

divergence. The leakage current is primarily due to carriers generated in the depletion region of the voltage blocking reverse biased PN junction. The leakage current in IGBTs can be expressed as:

$$J_L = \frac{n_i}{\tau_{SC}} \sqrt{\frac{2q\varepsilon_{si} V_{CE}}{N_D}} \frac{1}{(1-\alpha_{PNP})} \tag{3.59}$$

Where V_{ce} is the OFF-state voltage, τ_{sc} is the space charge generation lifetime, N_D is the doping of the voltage blocking drift layer and α_{PNP} is the open-base current gain of the PNP BJT within the IGBT. The carriers generated in the depletion region are multiplied by the gain of the PNP BJT. The intrinsic carrier concentration increases with temperature thereby causing a positive temperature coefficient for the leakage currents. For series connected IGBTs with different levels of leakage current, the device with the higher leakage current sets the overall leakage current, hence, the device with the lower leakage current needs to adjust its internal electric field distribution to supply the carriers required to maintain the overall level of leakage. This means that the device with the lower leakage current supplies a greater than normal number of carriers to maintain the flow of leakage current, hence, the device becomes more depleted thereby blocking a higher magnitude of OFF-state voltage. The blocking voltage and its temperature derivative is given by [3]:

$$V_{CE} = \frac{N_D}{2q\varepsilon_{si}} \left(J_L \frac{\tau_{SC}}{n_i} (1-\alpha_{PNP}) \right)^2 \tag{3.60}$$

$$\frac{dV_{CE}}{dT} = -\frac{N_D}{q\varepsilon_{si}}\left(J_L \frac{\tau_{SC}}{n_i}\left(1-\alpha_{PNP}\right)\right)^2 \frac{1}{n_i^3}\frac{dn_i}{dT} \tag{3.61}$$

The temperature dependent intrinsic carrier concentration, space-charge generation lifetime and the gain of the PNP BJT within the IGBT determines the blocking voltage given a defined leakage current. The IGBT with the higher junction temperature has a higher intrinsic carrier concentration and thus, a lower blocking voltage. Fig.3.36 (a) shows the OFF-state voltage sharing between two series connected IGBTs with two different junction temperatures (85 ˚C and 135 ˚C). As can be seen, the device with higher junction temperature has lower blocking voltage. Fig.3.36 (b) compares the voltage sharing of the series connected SiC MOSFETs at two different junction temperatures. As can be seen, SiC MOSFET is less sensitive to the temperature variation and hence, it shows a more balanced voltage sharing. This is due to the wide bandgap of the device which reduces the impact ionization of the carriers which is the main mechanism determining the voltage sharing during the reverse blocking of the device.

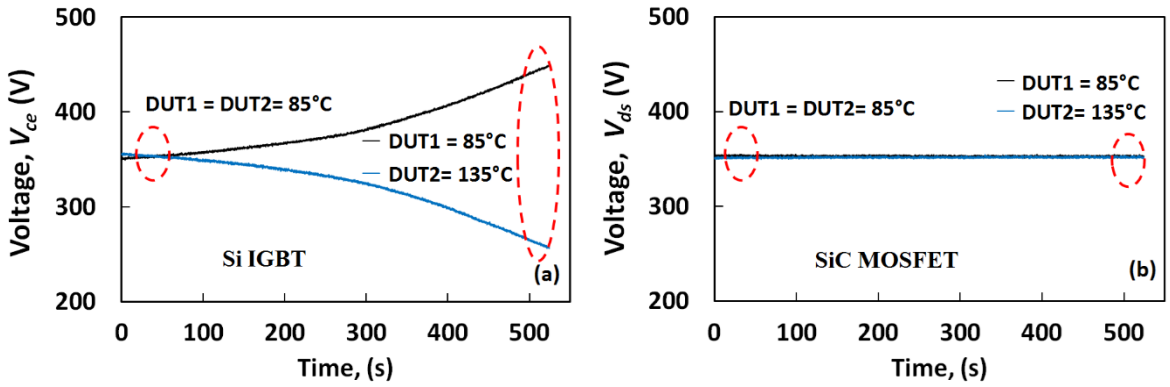

Fig. 3.36 OFF-state voltage sharing of two series connected devices with temperature mismatch: a) Si IGBT b) SiC MOSFET.

In designing the power stage with series connected devices, a snubber resistor is used to ensure the voltage sharing during the off-state. The worst-case snubber resistor size is dependent on the maximum leakage current of the devices used in series [12]:

$$\hat{R} \leq \frac{nV_D - V_S}{(n-1)\hat{I}_b} \tag{3.62}$$

In the datasheet of power devices, the values of leakage current are usually shown as a minimum, typical and maximum values, and the temperature dependency of them are not illustrated. This makes the optimization of the snubber sizing more challenging. In addition, as the power converter undergoes numbers of cycles, the tolerances of the snubbers degrades and this degradation on tolerances needs to be considered at the design phase which is out of the scope of this thesis. However, it can be seen from the equation that the series connected SiC MOSFET would inherently require larger snubber resistors for the OFF-state voltage balance which makes them more desirable due to the lower OFF-state snubber losses. For technology comparison the same devices

as named in the ON-state were selected and the reverse leakage current of them were measured at different temperatures. As shown in Fig.3.37 (a), with the rise of temperature, the leakage current increases throughout the whole range of voltage for Si IGBT. Moreover, the breakdown voltage of the device increases with the temperature. The qualitative explanation of this phenomena is that the hot carriers passing through the depletion layer under a high electric field lose part of their energy to optical phonons via scattering, resulting in a smaller ionization rate. Therefore, the carriers lose more energy to the crystal lattice along a given distance at a constant field. Hence, they must pass through a higher electric field before they can have enough energy for the impact ionization and generation of an electron-hole pair. In case of SiC MOSFET as shown in Fig.3.37 (b), the breakdown voltage is shifted to higher voltage with increase of temperature, however, the leakage current is less affected by the temperature and this is the main reason that the series connected SiC MOSFETs show a better voltage sharing during the OFF-state.

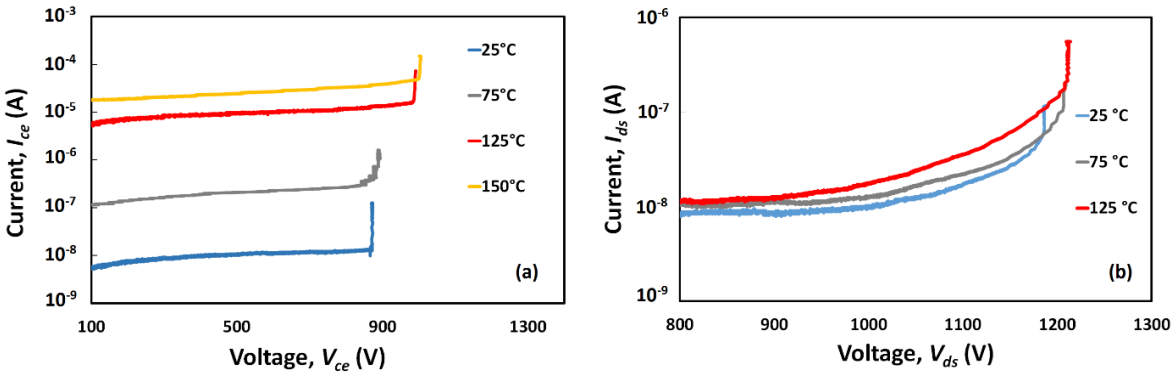

Fig. 3.37 Measured leakage current: (a) IGBT, (b) SiC MOSFET.

As explained earlier, the device with lower junction temperature blocks a higher voltage. Moreover, it was shown that the breakdown of the cooler device is lower. This dictates that the device needs to operate closer to the breakdown voltage region. Hence, it is important to investigate the impact of temperature on the leakage current and the voltage sharing especially for the recent snubberless active gate drive applications [13-15].

3.6 Conclusion

In this chapter the on-state and off-state voltage sharing of power devices was considered. The chapter starts with explaining the physics of power devices under ON and OFF state conditions. It was shown that the zero-temperature coefficient of the power devices determines the voltage sharing and loss distribution in the ON-state while the leakage current and switching synchronization is critical in the OFF-state. The comparison between the voltage sharing of SiC MOSFET and IGBT, as well as SiC Schottky and PiN diodes was done in this chapter. As discussed, if the current is above the ZTC, then the voltage drop across the hotter device is higher for both technologies. However, the difference is that ZTC of SiC MOSFET is significantly smaller. It was concluded that when the load current is below the ZTC, the forward voltage decreases with time due to increased lattice heating. This means that the IGBT dissipates less power as the device gets hotter. On the other hand, if the load current is above the ZTC, the forward voltage increases over time. This increases the power dissipation and the

junction temperature until it reaches steady state when the rate of heat generation becomes equal to the rate of heat extraction. Also a compact electrothermal model of two series Si IGBT and SiC MOSFET was developed in Matlab/Simulink. The model consists of 2 series connected devices with variable junction to case thermal impedances (Z_{th}). It was shown that the model precisely replicates the experimental results.

3.7 References

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Chapter

4 Dynamic Voltage Sharing in Series Connected Devices

4.1 Introduction

Voltage balancing during the turn-OFF of series connected devices is a very important consideration since voltage imbalance during turn-OFF can have potentially destructive consequences not just for the devices but for the entire converter. This is because voltage divergence between series connected devices can cause individual devices to exceed their maximum voltage limit thereby undergoing dynamic avalanche and potentially electrothermal failure if there is sufficient time for latch-up to occur [1, 2]. This problem is more acute for IGBTs than MOSFETs because of the bipolar nature of IGBTs. The MOSFET current is turned-OFF at a rate that depends on the electrical time constant (which depends on the Miller capacitance and total gate resistance) while the added complexity of minority carrier lifetime in the IGBTs makes IGBT turn-OFF more complicated and less predictable under series connected. Ideally, if the devices have identical parameters (threshold voltage, gate resistances etc.) and the gate drives are perfectly synchronized, then the total voltage during turn-OFF will be perfectly

balanced. However, imperfections and variations in devices and gate drivers means this is not the case. Traditionally, capacitive snubbers were designed to limit the total turn-OFF voltage commutation rate and ensure dynamic voltage sharing [3], however, this is at the expense of snubber losses, increased switching losses and a more bulky and expensive converter [4]. Active gate driving therefore seeks to dispense with the snubber by using an active gate controller to adjust the power devices gate drive voltage during switching [5,6]. The aim of this chapter is to present simulation and experimental results on the latest generations of series connected silicon IGBTs and SiC MOSFETs. Further insight is given into the voltage sharing performance of the devices when variations between the series devices are forced. In the analysis presented here, series connected devices are driven with different electrical time constants and are subjected to different junction temperatures.

4.2 Physics of Power Devices during Turn-OFF

4.2.1 Physics of IGBT Turn-OFF

Since power IGBTs are bipolar devices that rely on conductivity modulation to deliver low conduction losses, turning the device OFF usually involves the extraction of both

electrons and holes. Turning OFF the IGBT involves a rise in the V_{CE} to the DC voltage across the device and a fall in the I_{CE}. Fig. 4.1 (a) below shows finite element simulations of the IGBT turn-OFF voltage and current transient waveforms performed in SILVACO [7]. In the simulation, the IGBT is commutating current from a free-wheeling diode of an inductive load. Fig. 4.1 (b) shows the clamped inductive circuit used in the simulation together with the idealized waveforms expected from the simulations and measurements. The first pulse is used to charge the load inductance while the second pulse is used to evaluate the switching transient of the power device at turn-ON and turn-OFF. During the OFF state of the power device, current commutates through the free-wheeling diode. This is the classical clamped inductive switching circuit and is mostly used because it correctly emulates a single phase of the power converter driving an inductive load (for example the stator windings of an electrical machine in a drive application). Fig. 4.2 (a) to (f) show the V_{GE}, I_{GE}, V_{CE}, I_{CE}, P and T_J waveforms extracted from the simulator. The waveforms have been divided into 5-time phases.

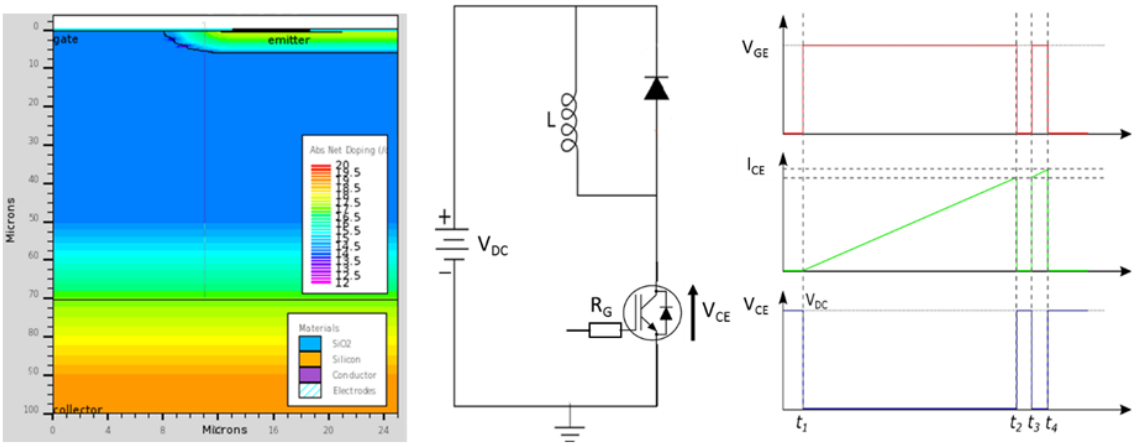


Fig. 4.1 (a) Finite element model of the silicon IGBT simulated in SILVACO. (b) Classical double pulse test used to extract the switching characteristics of power devices.

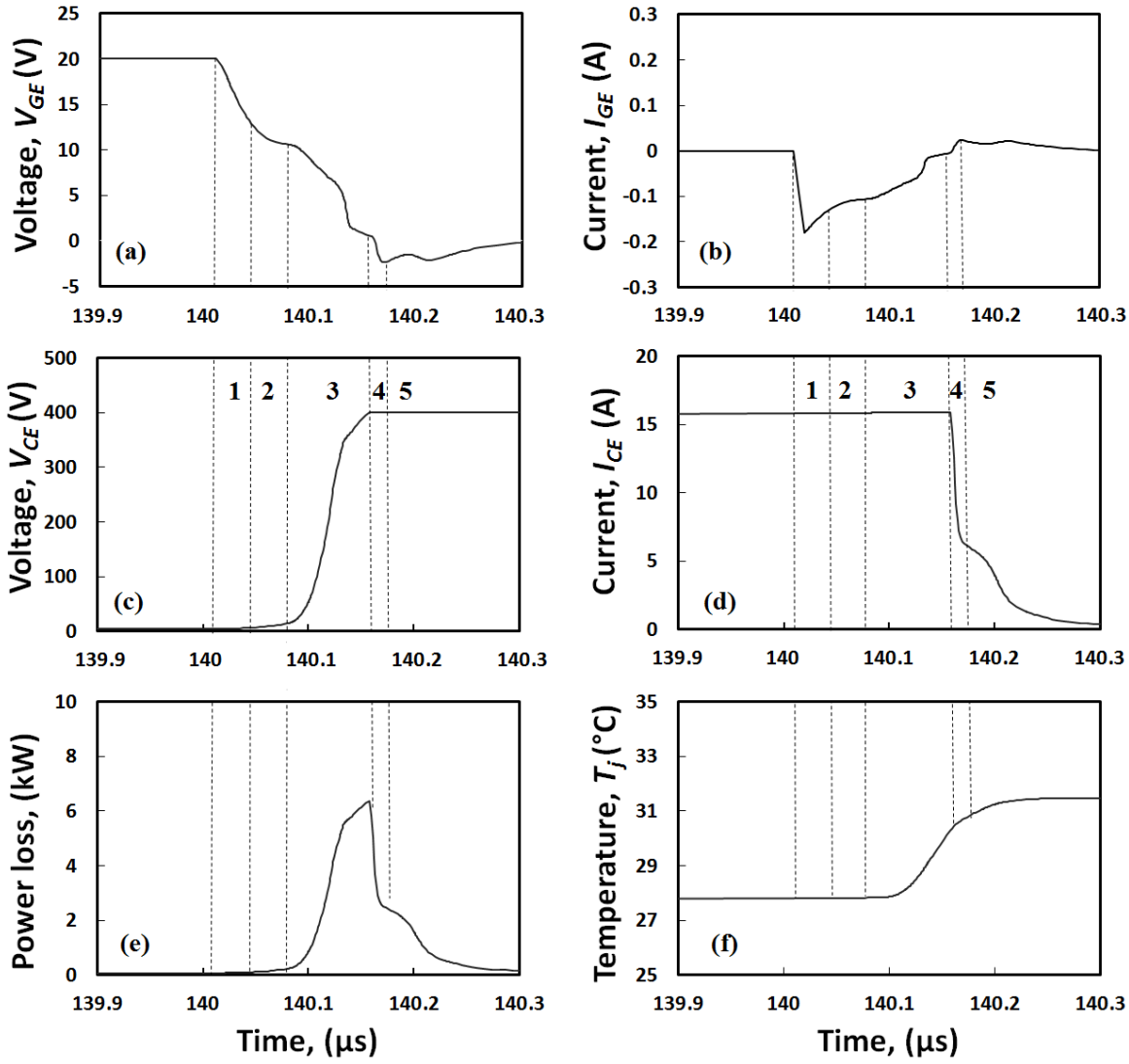


Fig. 4.2 (a) IGBT turn-OFF voltage transient (b) turn-OFF current transient (c) turn-OFF collector voltage transient (d) turn-OFF collector current transient (e) turn-OFF Instantaneous power dissipation (f) Junction Temperature.

Phase 1: The gate driver has issued the turn-OFF signal thereby discharging the gate-emitter capacitance (C_{GE}) of the IGBT. The V_{GE} voltage starts dropping from the ON-state voltage (between 15 and 20 V). The V_{CE} voltage remains in the ON-state, which depends on the conduction loss performance of the IGBT. The IGBT collector current is

still at the full load current and is supported by the electron current from the MOS channel and the hole current from the collector injection. The power loss is still dominated by the conduction loss (less than 0.5 kW) and the power dissipation is low.

Phase 2: The IGBT gate voltage goes into the Miller voltage or the Miller plateau. This simply means that gate current supplied from the gate driver is held constant while the collector-to-gate (C_{GC}) capacitance is charged. This Miller capacitance comprises of a series combination of the oxide capacitance (from the MOS gate) and the depletion capacitance. The oxide capacitance depends on the thickness, area and permittivity of the gate dielectric (which is SiO_2) and the depletion capacitance depends on the depletion width formed by the reverse bias voltage blocking PN junction. For reasons that will be explained later regarding minority carrier lifetime in the voltage blocking drift region, only the oxide capacitance is charged. During this phase, the collector current is still comprised of the full load current and the collector voltage is rising gradually due to the increased resistance of the channel. It should also be noted that the collector current is still comprised of electrons from the MOS channel and holes injected from the p+ collector. During this phase, the power dissipation is rising slowly (as seen in Fig. 4.2) and junction temperature starts to rise (as seen in Fig. 4.2).

Phase 3: Here the V_{GE} voltage drops below the threshold voltage of the MOS channel. Since the MOS channel is no longer inverted, the electron flow ceases. The collector current is then comprised solely of the hole current injected from the p+ collector, which at this point is sufficient to sustain the entire load current. The increased resistance resulting from the closed off MOS channel causes the collector voltage to start rising

which means that the depletion width of the voltage blocking junction starts to extend from the p-body junction towards the collector p+ junction. There is significant power dissipation (up to 6 kW) in this phase of the IGBT turn-OFF process as can be seen in Fig. 4.2, hence, the junction temperature rises rapidly.

Phase 4: The gate voltage V_{GE} falls to zero and the IGBT collector voltage reaches the DC link voltage which is set by the application. In most measurements, the presence of parasitic inductance along the path of current flow means that the IGBT collector voltage will overshoot the DC link voltage by an amount that depends on the current switching rate and the magnitude of the parasitic inductance. The rate at which the collector voltage changes will depend on the expansion rate of the depletion width, which in turn, depends on the concentration of minority carriers in the voltage blocking drift region. The concentration of minority carriers will depend on the lifetime which in turn will depend on processing parameters and junction temperature. At this stage, all of the supply voltage now falls across the initially free-wheeling diode shown in the clamped inductive switching circuit. In most cases, the diode capacitance would have been discharged, hence, the diode starts conducting current and commutating it away from the IGBT. Hence, the current through the IGBT starts to fall once the collector voltage of the IGBT reaches the supply voltage. There is significant power dissipation and junction temperature rise during this phase because of the simultaneously high collector voltage and current as shown in Fig. 4.2.

Phase 5: The IGBT gate voltage is fixed at zero while the collector voltage is clamped at the DC input voltage. The current falls until it reaches the tail current. The tail

current is due to the residual holes in the drift region that can only be extracted not by the expanding depletion width but by the recombination of minority carriers. Hence, the magnitude and duration of the tail current depends on the minority carrier lifetime. This is one significant disadvantage of IGBTs (compared to MOSFETs) in that there is additional losses due to the tail current since the collector voltage is high during this phase.

Fig. 4.3 (a) shows the simulated IGBT device with a vertical cutline while Fig. 4.3 (b) shows the hole carrier concentration taken across the vertical cutline while Fig. 4.3 shows corresponding electric field extracted from the simulator.

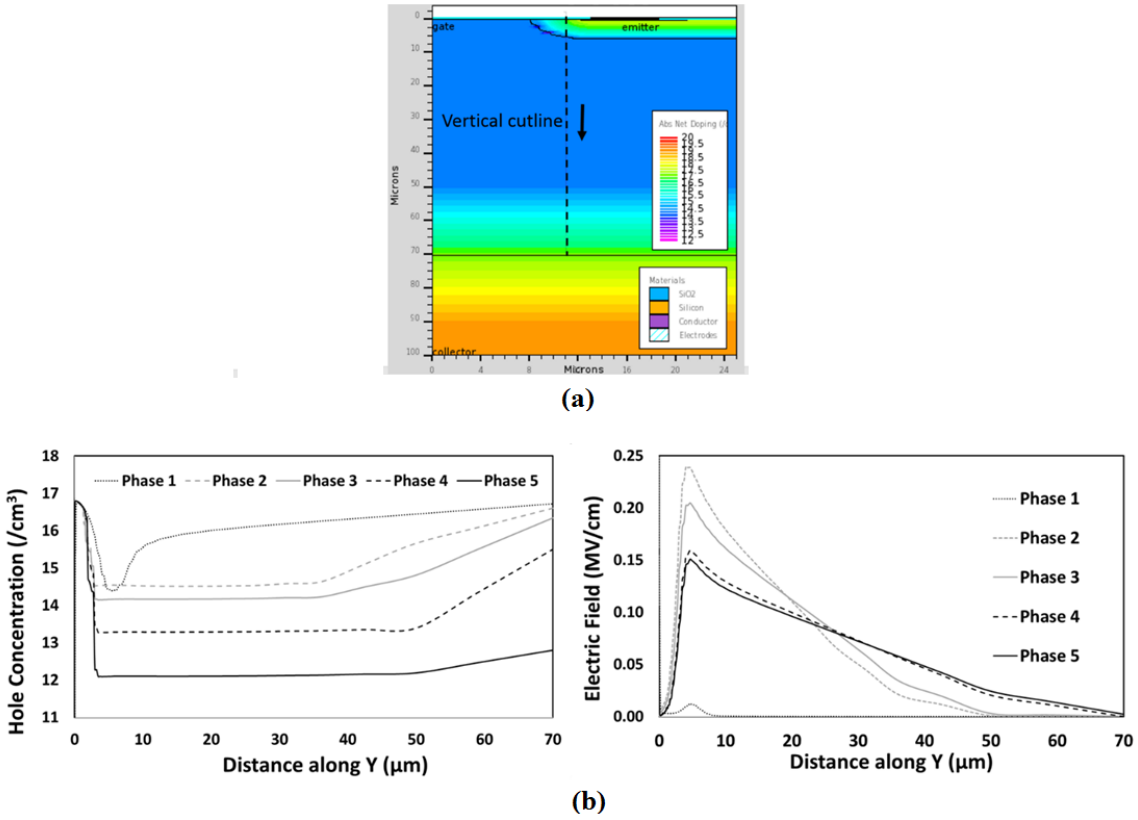


Fig. 4.3 (a) Simulated IGBT device (b) Hole carrier concentration in the drift region (c) The simulated electric field across the drift region

From the figures shown above, the hole carrier concentration decreases as the time phase progresses from phase 1 to 5. Likewise, the lateral extension of the electric field expands as the time phase progresses. This simulates the extension of the depletion width across the drift region as the IGBT is switched from ON-state to OFF-state.

4.2.2 Derivation of the IGBT Turn-OFF Voltage Commutation Rate.

The commutation rate of the collector voltage can be derived from first principles which will be shown below. In the derivation presented here, the gate voltage has already been turned OFF and the main rise of the collector voltage is due to carrier extraction from the drift region. Hence, the rate of carrier extraction is proportional to the rate at which the depletion width extends from the main voltage blocking PN junction to the p+ collector junction. The collector current of the IGBT. Consider a quantity of charge Q within a volume V defined by $A \cdot l$ where A is the area orthogonal to the direction of charge flow and l is the length in the direction of charge flow.

$$I = \frac{Q}{t}, \text{ where } Q = pqAl \tag{4.1}$$

$$I = \frac{pqAl}{t} = pqAv_d \tag{4.2}$$

Note that t has been substituted by l/v_d where l is the length covered by the moving charge and v_d is the drift velocity. Note that the drift velocity can be expressed as

$$v_d = \mu E \tag{4.3}$$

The equation for the current density is therefore derived as

$$J = \frac{I}{A} = pq\mu E \text{ or } J = \sigma E \tag{4.4}$$

where $\sigma = pq\mu$

In the context of the IGBT, as the MOS channel is switched OFF, the remaining carriers in the drift region must be extracted by the expansion of the depletion width and the recombination of the remaining carriers. The rate at which the MOSFET channel cuts-off current flow depends on the electrical time constant defined by the Miller capacitance and the gate resistance. The rate at which depletion width expands will depend on the minority carrier lifetime, which in turn depends on temperature. Both the turn-OFF rate of the MOS channel and the minority carrier lifetime will determine the voltage commutation rate of the IGBT as it is switched OFF. Hence, the expansion rate of the depletion width will be equal to the drift velocity of the carriers contributing to the collector current.

$$I = nqAv_d = pqA\frac{dW}{dt} \tag{4.5}$$

To relate the equation above to the voltage commutation rate, we must first start from Gauss's law of electricity

$$\int E \cdot dA = \frac{Q}{\varepsilon_0 \varepsilon_r} \tag{4.6}$$

The total charge in the drift layer can be expressed as

$$Q = q(N_D + p_{SC})WA \tag{4.7}$$

where N_D is the doping concentration (in cm^{-3}) of the drift layer, p_{sc} is the hole charge concentration (in cm^{-3}) in the drift layer and W is the total width of the depletion layer. Hence, Gauss law for an IGBT under turn-OFF, can be re-written as

$$\frac{dV}{dW} = \frac{q(N_D + p_{SC})W}{\varepsilon_0 \varepsilon_r} \tag{4.8}$$

where the electric field has been replaced by dV/dW. Using the chain rule, equation (4.8) can be re-written as:

$$\frac{dV}{dt}\frac{dt}{dW} = \frac{q(N_D + p_{SC})W}{\varepsilon_0 \varepsilon_r} \tag{4.9}$$

$$\frac{dV}{dt} = \frac{q(N_D + p_{SC})W}{\varepsilon_0 \varepsilon_r}\frac{dW}{dt} \tag{4.10}$$

Combining equation (4.5) with equation (4.10) yields

$$\frac{dV}{dt} = \frac{(N_D + p_{SC})W}{\varepsilon_0 \varepsilon_r}\frac{I}{pA} \tag{4.11}$$

To get the final expression of the voltage commutation rate as a function of the supply voltage, we have to expression the depletion width as a function of the collector voltage. By integrating equation (4.8) we can get the depletion width as a function of the collector voltage:

$$\int_0^{V_C} dV = \frac{q(N_D + p_{SC})}{\varepsilon_0 \varepsilon_r}\int_0^{W} W dW \tag{4.12}$$

$$V = \frac{q(N_D + p_{SC})W^2}{2\varepsilon_0 \varepsilon_r} \tag{4.13}$$

$$W = \sqrt{\frac{2q\varepsilon_0 \varepsilon_r V}{(N_D + p_{SC})}} \tag{4.14}$$

Substituting equation (4.14) into equation (4.11) yields the final equation for the voltage commutation rate of the IGBT as a function of the collector current and the collector voltage.

$$\frac{dV}{dt} = \sqrt{\frac{2q(N_D + p_{SC})V}{\varepsilon_0 \varepsilon_r}} \frac{I_C}{pA} \tag{4.15}$$

It can be seen from equation (4.15), that the collector voltage commutation rate increases with increasing collector current and voltage, however, crucially, it increases with decreasing hole carrier concentration. This means that there is a temperature and lifetime dependency of *dV/dt* since the hole concentration increases with carrier lifetime and temperature.

Impact of Gate Resistance: The gate resistance used to drive an IGBT will have direct control over the rate at which the MOS channel is formed or cut-off. However, the actual current and voltage commutation rates during turn-OFF depend on the rate at which the hole minority carriers are extracted from the drift region. This depends on hole lifetime which in turn is dependent on temperature and the lifetime treatment (done during fabrication). Finite element simulations of silicon IGBTs have been performed with different gate drive resistances. Fig. 4.4 (a) to (f) shows the impact of the gate resistance on the gate voltage, gate current, collector voltage, collector current, power dissipation and junction temperature. It can be seen from the figures that increasing the gate resistance slows down the gate voltage (V_{GE}) commutation rate, which in turn delays the time instant where the gate voltage falls below the threshold voltage. Therefore, the V_{CE} and I_C transients are shifted rightwards (delayed). Looking at the

power dissipation comparison between the slow and the fast IGBT transients, it can be concluded that there is marginal change in the total loss as the gate resistance is varied. When the gate resistance is reduced, the peak gate current increases although the total gate charge remains constant.

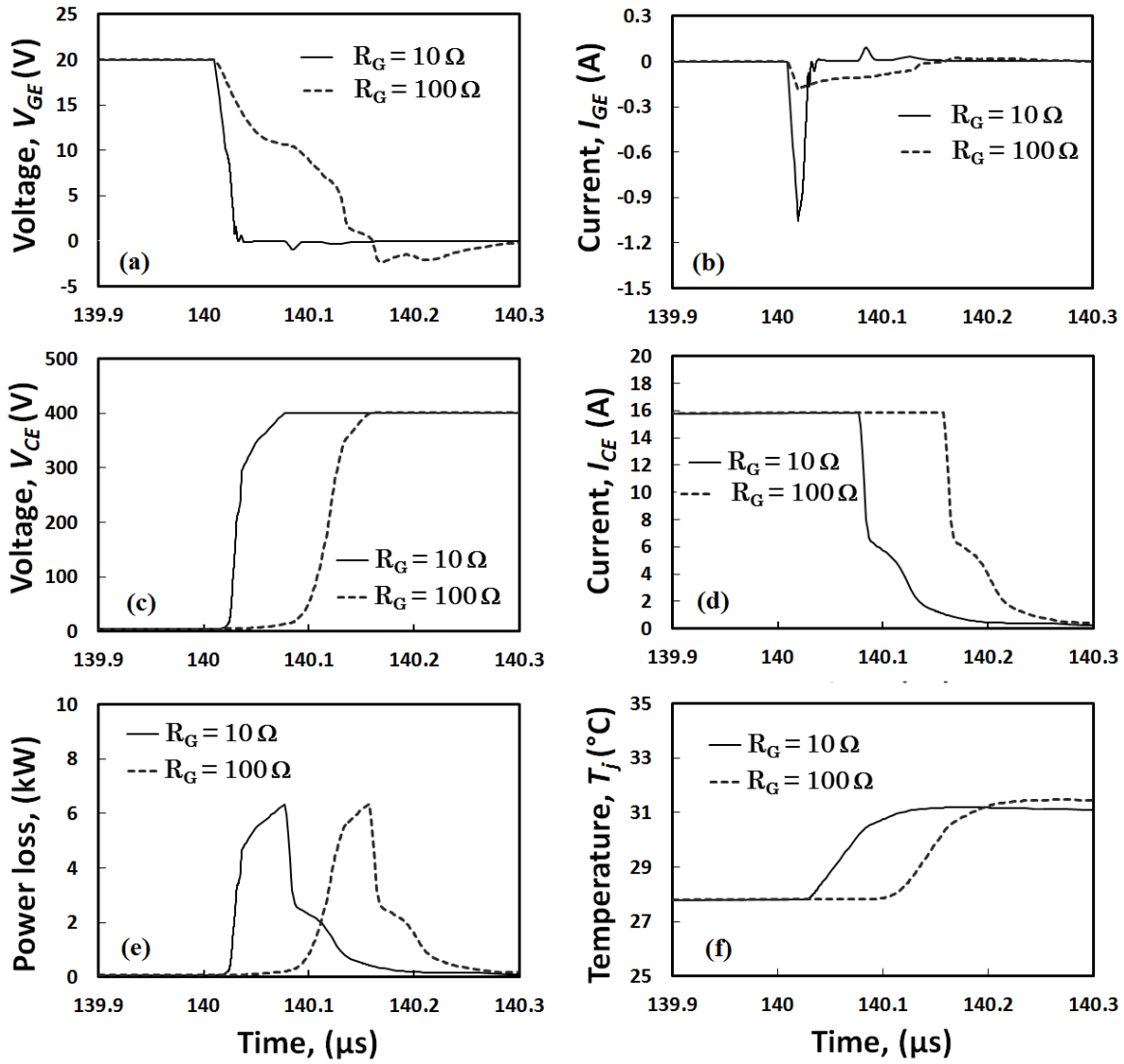


Fig. 4.4 Impact of the gate resistance on the (a) V_{GE} transient (b) I_{GE} transient (c) V_{CE} transient (d) I_C transient (e) Power dissipation and (f) Junction temperature.

Experimental measurements have been obtained from 1.2kV/30A silicon IGBTs which have been switched at different gate resistances (R_G = 10 Ω. 100 Ω and 180 Ω). Fig. 4.5 (a) shows the turn-OFF current transient while Fig. 4.5 (b) shows the turn-OFF voltage transient. Similar to the simulations, the waveforms have been shifted rightwards in time as the gate resistance is increased. However, the actual voltage and current commutation rates have not changed appreciably with the gate resistance. This is because the gate resistance directly changes the electron current but not the hole current (which depends on temperature and lifetimes).

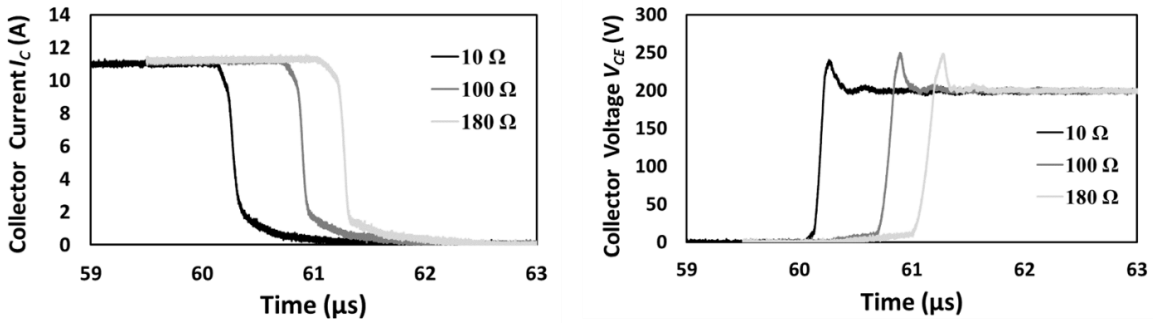


Fig. 4.5 Impact of the gate resistance on the (a) collector current and (b) collector current.

Impact of Junction Temperature: Fig. 4.6 shows the results of the finite element simulations comparing the turn-OFF transient of the same IGBT at different temperatures. As can be seen from Fig. 4.6, the device junction temperature does not have any appreciable impact on the gate voltage or gate current transient waveforms. However, the collector voltage and current waveforms are significantly impacted by temperature. As the equation for the dV_{CE}/dt correctly predicts, the voltage commutation rate reduces with temperature since the hole concentration lifetime in the

drift region increases. The tail current and turn-OFF power dissipation also increases with temperature as can be seen from Fig. 4.6 (e) and Fig. 4.6 (d). In conclusion, increasing the junction temperature of the IGBT slows down the voltage and current commutation rates because of the increased minority carrier lifetime.

Experimental measurements have also been performed on a 1.2kV/30A silicon IGBT from Fig. 4.7 which was switched at different temperatures. The turn-OFF transient waveforms of the collector voltage and current were extracted and shown in Fig. 4.7 (a) for the collector voltage and Fig. 4.7 (b) for the collector current. Similar to what was observed in the simulations, the turn-OFF voltage commutation rate decreases with increasing temperature and the tail current increases with temperature.

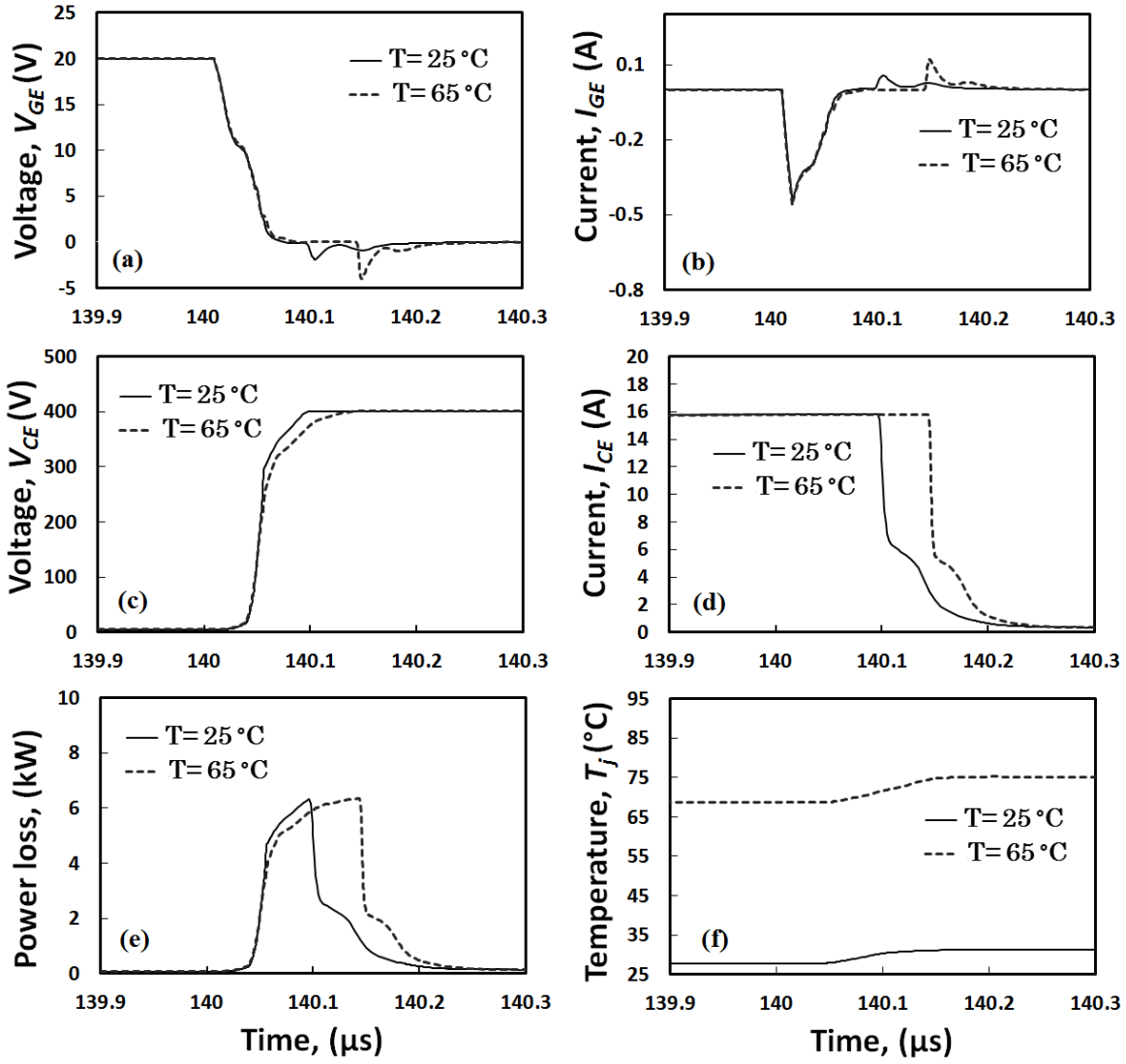


Fig. 4.6 Impact of the IGBT junction temperature on the (a) V_{GE} transient (b) I_{GE} transient (c) V_{CE} transient (d) I_C transient (e) Power dissipation and (f) Junction temperature.

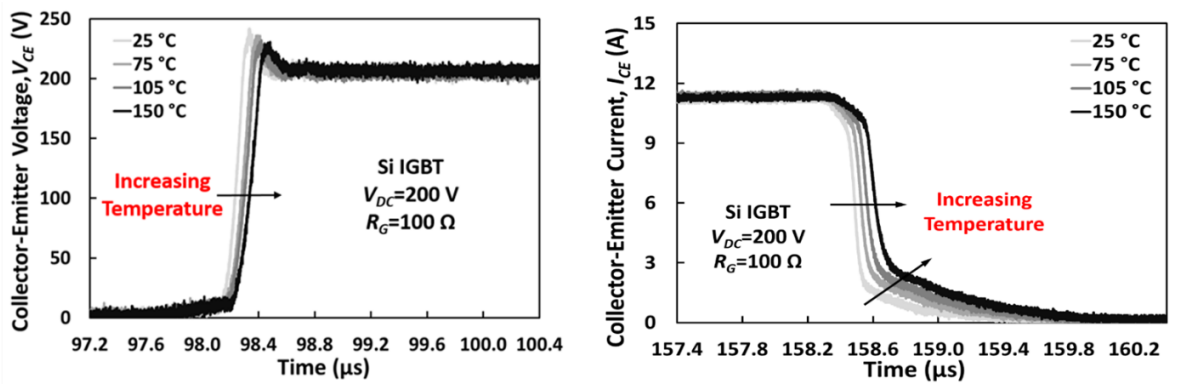


Fig. 4.7 Experimental measurements showing the impact of temperature on the turn-OFF transient (a) Collector voltage and (b) Collector current waveforms of a 1.2kV/30A silicon IGBT.

Impact of hole carrier lifetime: When a minority carrier diffuses through a semiconductor region, it eventually recombines with the majority carrier either through radiative recombination, SRH recombination or Auger recombination. In direct bandgap semiconductors like GaN, radiative recombination is the dominant recombination mechanism and is characterised by the release of a photon with a wavelength that depends on the bandgap. This is the basis of most photonic applications like LEDs and lasers. In the case of silicon IGBTs, the dominant recombination mechanism is SRH recombination and the time duration before the recombination process occurs is called the lifetime. IGBTs work on the principle of conductivity modulation which is based on electron-hole recombination occurring in the drift region during the ON-state. The electrons are injected from the MOS channel while the holes are injected from the forward biased collector p+ junction. Hence, as the hole concentration is increased, conductivity modulation is enhanced (which reduces conduction losses) however, the tail current is extended and switching losses are

increased. Fig. 4.8 (a) to (f) shows finite element simulations of 2 silicon IGBTs with different hole carrier lifetimes. It can be seen that the gate voltage and gate current transients are unaffected by the change in hole lifetime as expected. The collector voltage and current are however significantly affected with the increase in hole lifetime causes a decrease in the collector voltage commutation rate and extending the tail current of the turn-OFF current considerably. Hence, the turn-OFF switching power increases considerably with increased hole carrier lifetime. The junction temperature also shows a significant increase as the hole lifetime is increased.

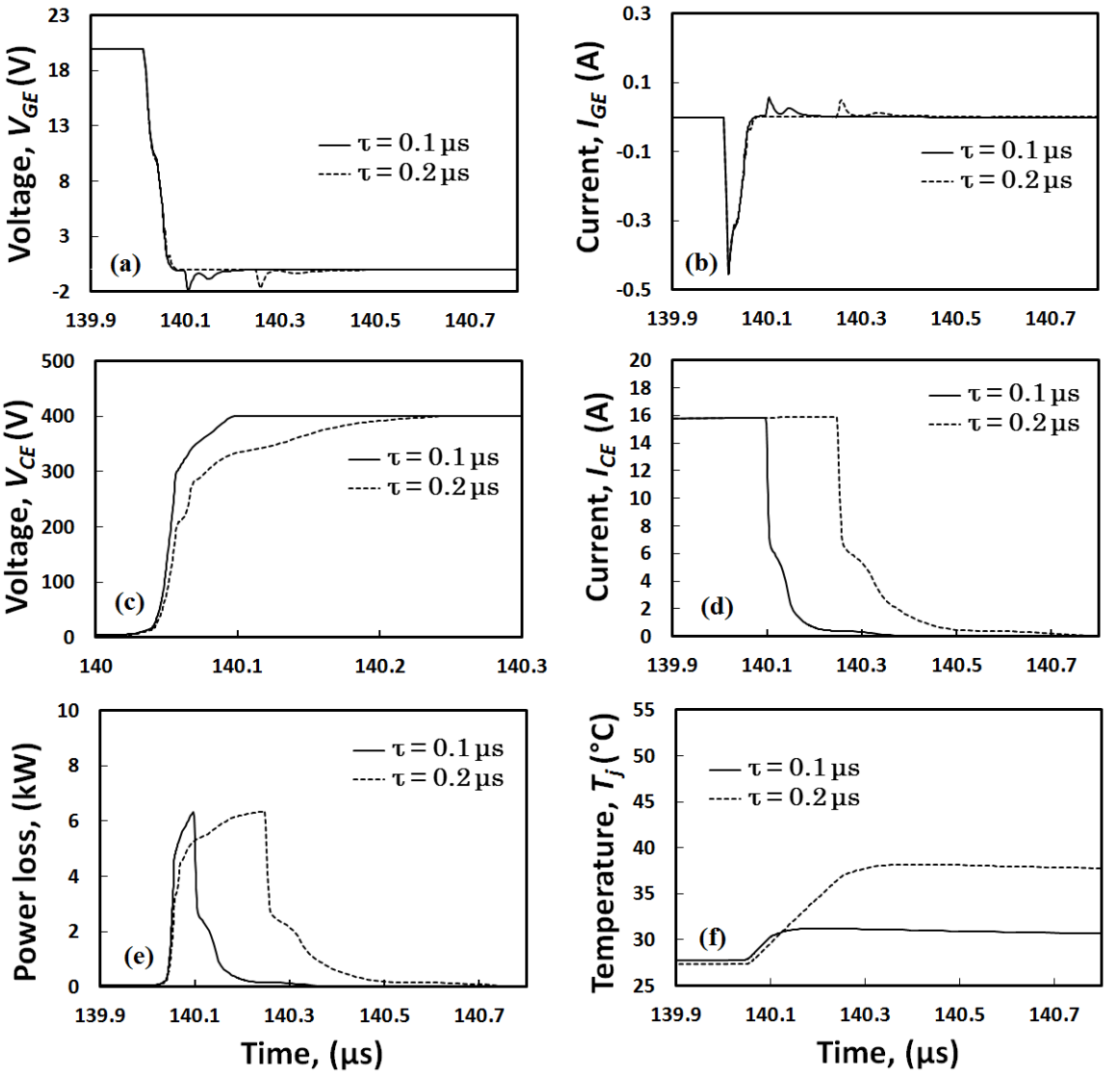


Fig. 4.8 Impact of the hole carrier lifetime on the (a) V_{GE} transient (b) I_{GE} transient (c) V_{CE} transient (d) I_C transient (e) Power dissipation and (f) Junction temperature.

4.2.3 Physics of MOSFET Turn-OFF.

MOSFETs are unipolar devices that conduct current through the drift of majority carriers, hence, current flow is due only to electron drift. This means there are no minority carrier effects like stored charge and tail currents due to minority carrier lifetime. Hence, MOSFET turn-OFF is governed solely by the charging of the output capacitance (C_{OSS}) which is the sum of the miller capacitance (C_{GD}) and the drain source capacitance (C_{DS}). The physics of MOSFET turn-OFF is considerably simpler than that of IGBT turn-OFF. Fig. 4.9 shows the simulated turn-OFF gate voltage and current as well as the drain voltage and current of the power MOSFET during turn-OFF of a clamped inductive switching arrangement.

Phase 1: The gate drive voltage issues the command to de-energise the gate, hence, the MOSFET gate voltage starts to fall from the recommended drive voltage. There is a peak current supplied by the gate driver as seen in Fig. 4.9. The drain current remains at the load current while drain voltage remains at the ON-state voltage which depends on the current and the ON-state resistance. The rate at which the V_{GS} falls will depend on the input capacitance of the MOSFET.

Phase 2: The gate voltage of the MOSFET falls to the Miller voltage (V_{GP}). During this phase, the gate drive current is charging the Miller capacitance and hence, the main voltage transient occurs. Unlike the case of the IGBT, the drain voltage depends entirely on the rate at which the Miller capacitance is charged. By the end of the Miller

voltage plateau, the drain voltage has reached the DC link voltage. The current through the MOSFET is still at the load current because the channel in ON since V_{GS} is still higher than V_{TH}. There is significant power dissipation during this phase as shown in Fig. 4.9 (e).

Phase 3: The gate voltage falls below the threshold voltage thereby cutting off the channel and commutating current to the free-wheeling diode anti-parallel to the load inductance. The drain voltage remains at the DC link voltage.

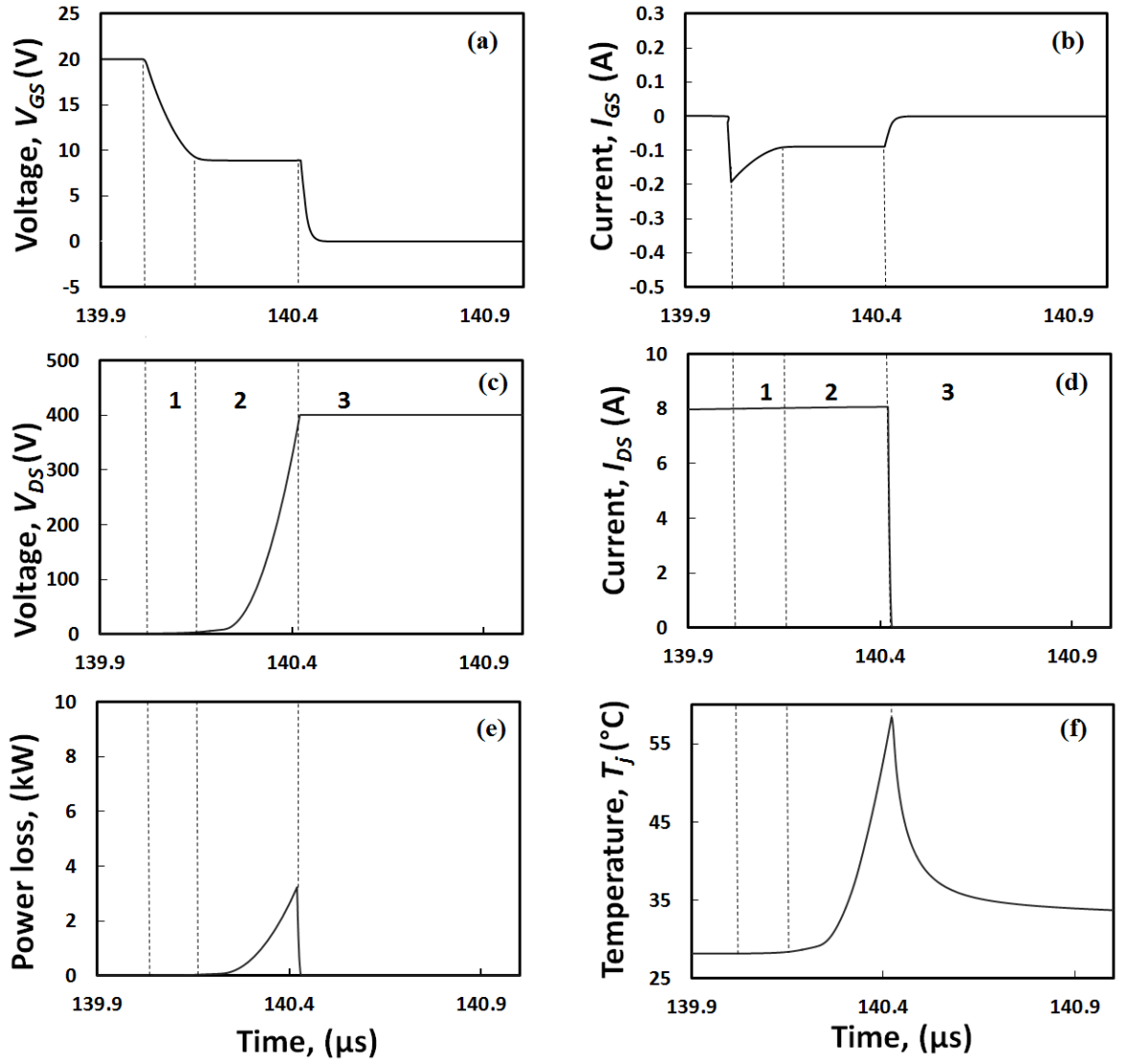


Fig. 4.9 MOSFET Turn-OFF (a) V_{GS} transient (b) I_{GS} transient (c) V_{DS} transient (d) I_{DS} transient (e) Power loss and (f) Junction temperature.

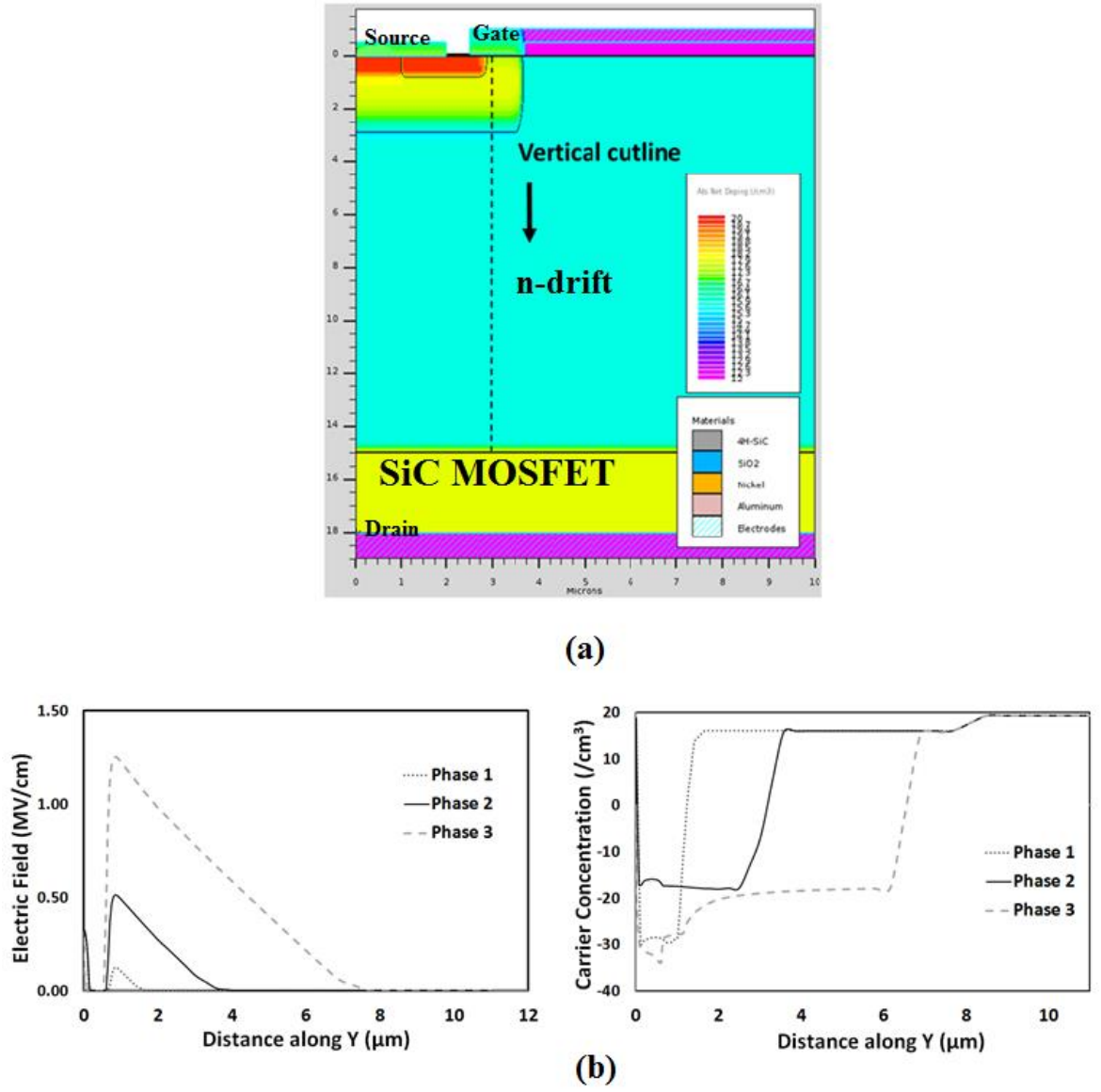


Fig. 4.10 (a) Simulated SiC MOSFET device (b) The simulated electric field across the drift region and Hole carrier concentration in the drift region

Fig. 4.10 (a) shows the simulated SiC MOSFET device with a vertical cutline while Fig. 4.10 (b) shows the hole carrier concentration taken across the vertical cutline, also Fig. 4.10 (b) shows corresponding electric field extracted from the finite element modelling.

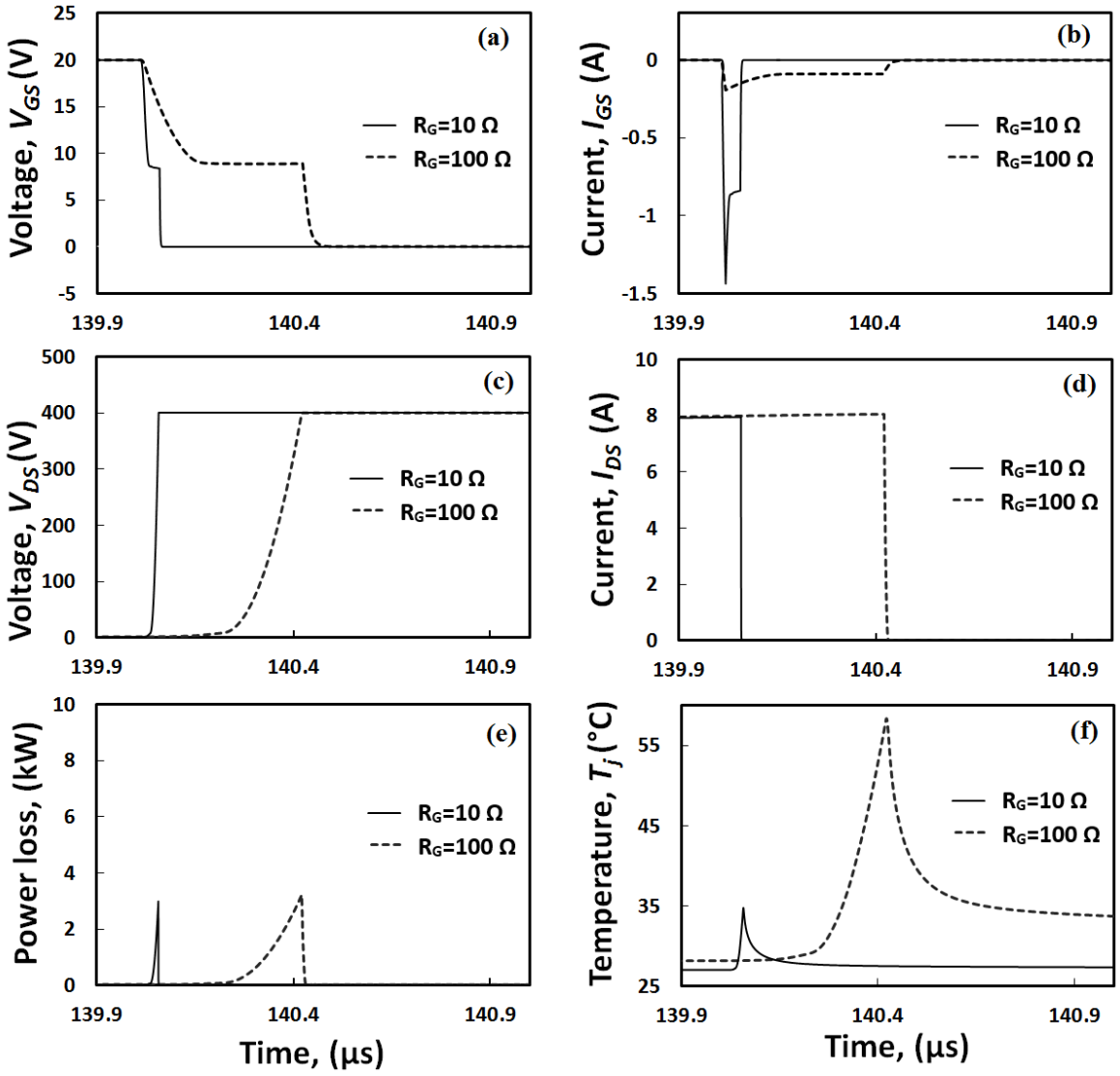


Fig. 4.11 Impact of the gate resistance on the (a) V_{GS} transient (b) I_{GS} transient (c) V_{DS} transient (d) I_{DS} transient (e) Power loss and (f) Junction temperature.

Fig. 4.11 (a) to (f) shows the impact of the gate resistance on the gate voltage, gate current, collector voltage, collector current, power dissipation and junction temperature. As shown, the plateau region of the gate voltage extends with increasing

the gate signal. This in return reduces the drain source voltage build up and can increase the power losses during the switching events.

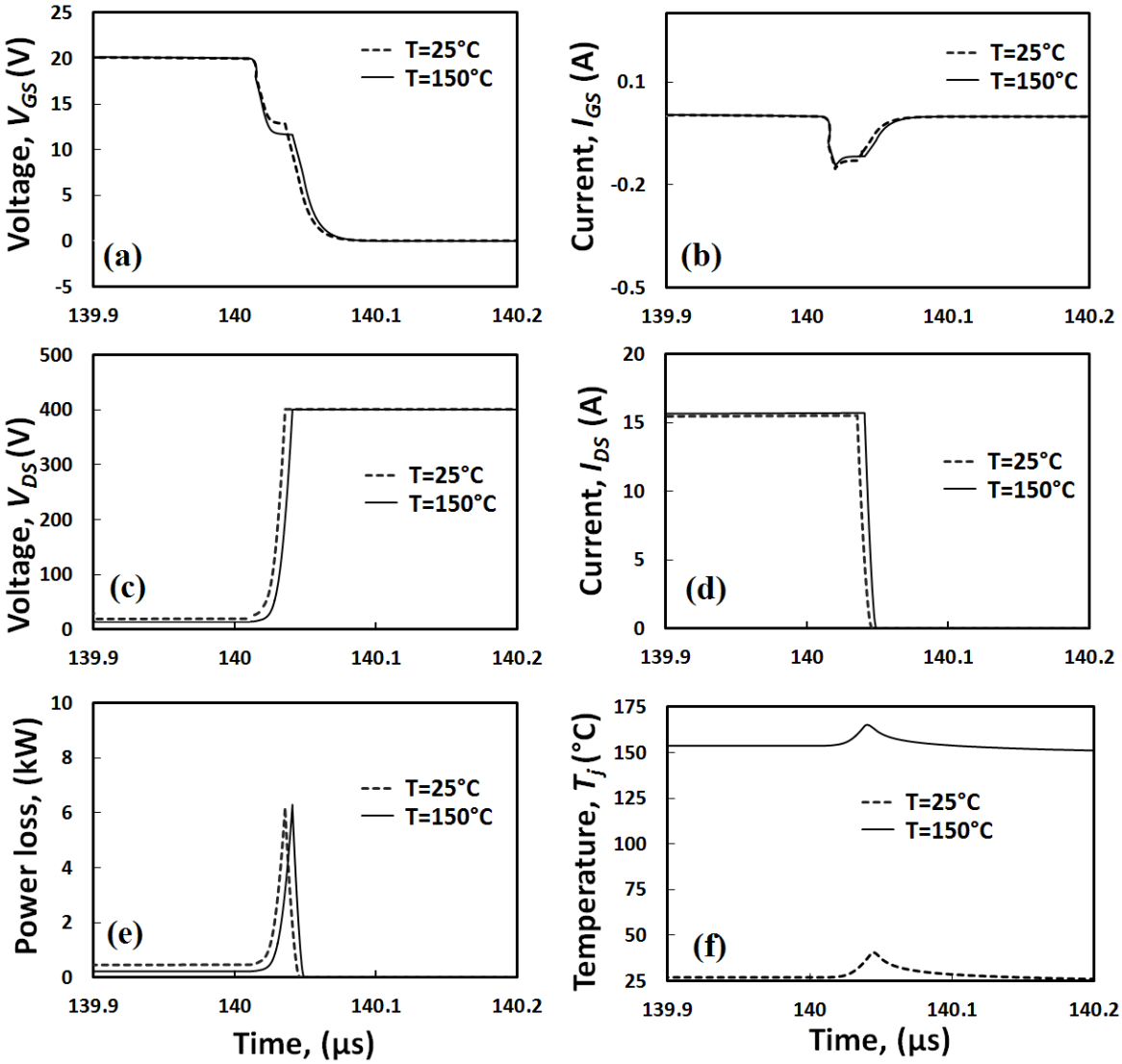


Fig. 4.12 Impact of SiC MOSFET junction temperature on (a) V_{GS} transient (b) I_{GS} transient (c) V_{DS} transient (d) I_{DS} transient (e) Power loss and (f) Junction temperature.

Fig. 4.12 shows the results of the finite element simulations comparing the turn-OFF transient of the same SiC MOSFET at different temperatures. Increased temperature, increases the plateau at the gate voltage and reduces the threshold voltage. This marginally increases the losses during the switching.

4.2.4 Derivation of MOSFET Voltage Commutation Rate

The displacement current of the depletion capacitance is given by:

$$I_{GD} = C_{GD} \frac{dV_{GD}}{dt} \tag{4.16}$$

During the plateau period, the gate current can be represented as:

$$I_{GD} = \frac{V_{GP}}{R_G} \tag{4.17}$$

Combining both equations yields

$$\frac{dV_{GD}}{dt} = \frac{V_{GP}}{R_G C_{GD}} \tag{4.18}$$

where

$$V_{GP} = V_{TH} + \sqrt{\frac{LI_L}{W\mu C_{OX}}} \tag{4.19}$$

4.3 Finite Element Simulations of Dynamic Voltage Sharing in Series Power Devices

When power devices are connected in series, they share the same current, however, not the same voltage. This is unlike parallel connections where the same voltage is shared but not the same current. Dynamic voltage balancing in series connected power devices is a significant problem that has historically been solved using capacitive snubbers. The first HVDC-VSC converters commissioned by ABB were 2-level converters that used series connected power devices for voltage sharing. How well the devices share voltage will depend on the internal physics of the turn-OFF process.

4.3.1 Finite Element Modelling of Series IGBTs under Turn-OFF

Due to the bipolar nature of IGBTs, voltage sharing of series devices during turn-OFF is more complicated. Under ideal conditions, meaning there is no electrical or thermal variation between the series devices and the gate drivers are perfectly synchronized, then there is no voltage divergence. In other words, each IGBT will exhibit the same turn-OFF voltage transient and the total voltage will be perfectly balanced along the series link. However, there are unavoidable electrical and thermal variations between IGBTs and gate drivers inevitably exhibit unsynchronized switching. Variations in threshold voltages, minority carrier lifetime and internal gate resistance can cause significant differences in switching characteristics between IGBTs. Finite-element models have been developed to describe the physics behind the behaviour of series-connected silicon IGBTs under clamped inductive switching. The circuit shown in Fig. 4.13 has been simulated in ATLAS from SILVACO using the mixed mode circuit application to solve the switching transients with the finite-element model. Simulations have been performed to investigate the impact of (i) different switching rates, (ii) different junction temperatures and (iii) different hole lifetimes on series connected silicon IGBTs under clamped inductive switching conditions. Table 4.1 below details the parameters of the IGBT under simulation.

Table 4.1 Details of the finite element model of the silicon IGBT

Parameter	Value	Parameter	Value
Drift layer thickness (μm)	62	n^+ source doping (cm^{-3})	5×10^{20}
Drift layer doping (cm^{-3})	1.5×10^{14}	n^+ source depth (μm)	0.4
Oxide thickness (nm)	80	p- body depth (μm)	5.5
p-body doping (cm^{-3})	7×10^{16}	p+ doping (cm^{-3})	1×10^{17}
n-collector doping (cm^{-3})	1×10^{17}	Hole lifetime (μs)	1
Channel length (μm)	4	Electron lifetime (μs)	1
Breakdown Voltage (V)	900	Gate Resistance (Ω)	100
DC Link Voltage (V)	400	Load Current (A)	17

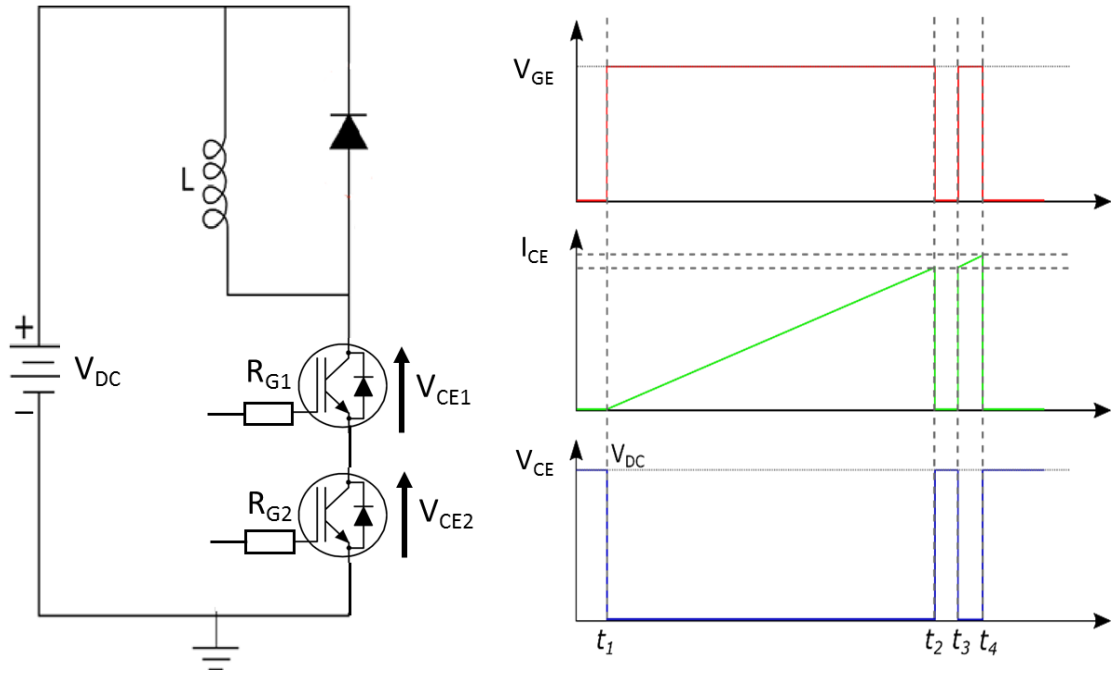


Fig. 4.13 Clamped inductive switching circuit with series connected IGBTs.

Variation in Switching Rates: Fig. 4.14 shows the voltage sharing between two series

connected IGBTs which are switching at different rates. In this simulation, DUT1 is switching at a faster rate (R_G=100 Ω) than DUT2 (R_G=120 Ω). The simulations show that the faster switching IGBT undergoes an uncontrolled voltage rise while the slower switching IGBT's collector voltage collapses close to zero.

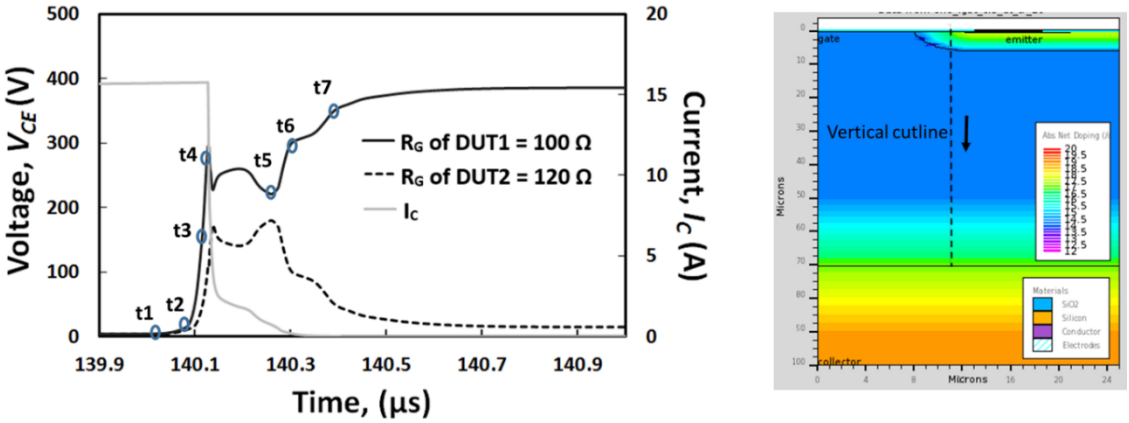


Fig. 4.14 Turn-OFF collector voltage and current in series connected silicon IGBTs switched with different gate resistances.

It can be observed from the transient characteristics in Fig. 4.14 that the uncontrolled voltage divergence occurs during the tail current phase of the turn-OFF current transient. As has been discussed earlier, the tail current phase of the turn-OFF transient is governed by the recombination of holes with electrons in the drift region of the power device. Since the MOS channel of the fast IGBT is closed OFF faster in the device with the lower gate resistance, the current through the faster device is supported by minority carrier recombination while the current in the slower device is still flowing through the channel. As a result, the voltage in the faster IGBT rises faster and to maintain the current flow, the depletion width extends further beyond where it should.

In other words, if current is forced to flow from a device that is depleted to its maximum rated depletion width, then the depletion width would be forced to extend further for the device to supply the necessary carriers to maintain the current flow. Since the voltage supported by the device is simply the integration of the electric field over the depletion width, then the fast switching IGBT that has to deplete further to maintain the same current flow, will block the higher voltage. The rate of voltage divergence increases during the tail current because that is where the main voltage commutation rate occurs as has been discussed previously. Fig. 4.15 shows the internal electric field in the fast and slow IGBTs (at 7 time instances that correspond to the labelled times t_1 to t_7 in Fig. 4.14) where the fast IGBT has a considerably higher internal electric field caused by the more rapid carrier recombination compared to the slow IGBT.

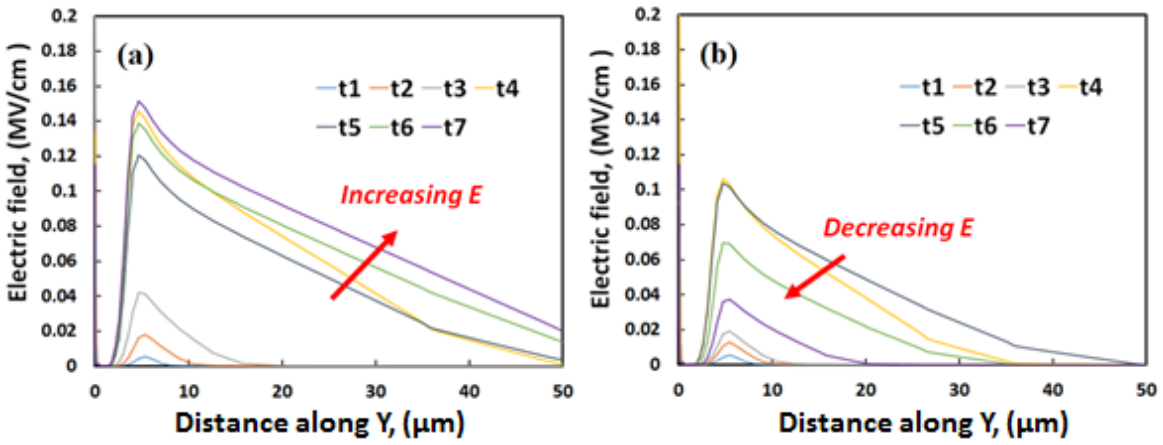


Fig. 4.15 Internal electric field in the drift region for the (a) Fast IGBT switched with 100 Ω and (b) slow IGBT switched with 120 Ω

The internal carrier concentrations across the drift region for both IGBTs can be compared by observing Fig. 4.16 which shows the carrier concentration profiles in the

drift region at times t_1 to t_7 corresponding to Fig. 4.14. It can be seen from Fig. 4.16 (a) that the drift region of the fast IGBT from time t_4 onwards becomes fully depleted of holes while that of the slow IGBT still exhibits significant hole concentration. This corresponds to the more rapid expansion of the electric field and depletion width in the faster switching IGBT. Hence, the slower switching IGBT, which sets the overall current flowing through both IGBTs forces the faster IGBT into further depletion to maintain the overall current flow.

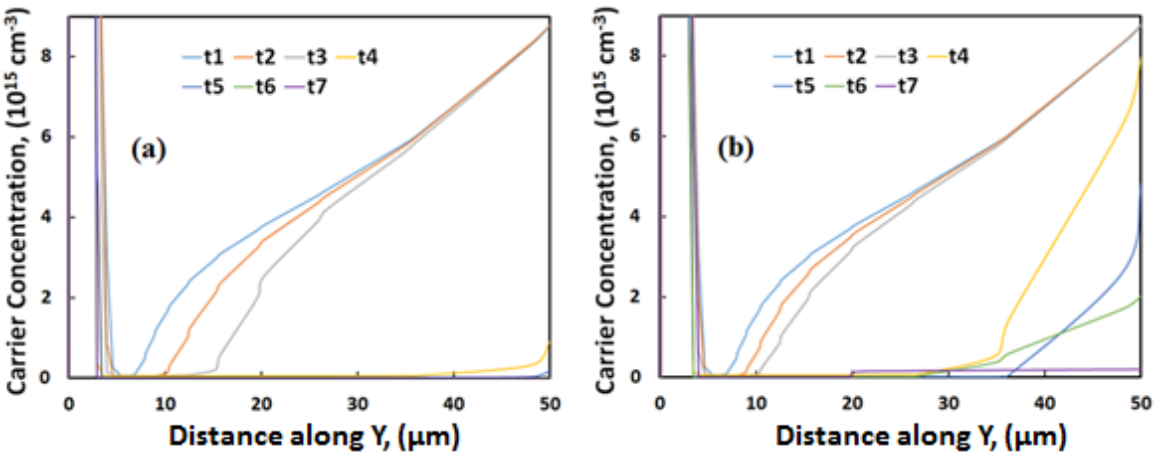


Fig. 4.16 Carrier concentration in the drift region for the (a) Fast IGBT switched with 100 Ω and (b) slow IGBT switched with 120 Ω.

Similar simulations of series connected IGBTs have been performed with differences in the junction temperature between the series devices. This scenario is simulated because it is not an unexpected practical condition in the actual converter. Differences in the junction temperature between series devices can be caused by defects in the cooling system and/or increased thermal resistance from thermo-mechanical power cycling degrading the devices at different rates. Differences in the rate of device

degradation between the series devices can cause different junction temperature. Increased contact resistance in the emitter wirebonds and increased solder pad delamination is known to contribute to increased junction-to-case thermal resistance thereby increasing the junction temperature of the device. Hence, it is important to understand the impact of this on voltage divergence between the series devices. Fig. 4.17 shows the voltage divergence in the turn-OFF waveforms of the series connected IGBTs with the lower junction temperature IGBT blocking the higher voltage. This is due to the reduced carrier lifetime (since hole lifetime with the drift region will increase with the junction temperature) meaning that the lower junction temperature device has a reduced hole concentration in the drift region at turn-OFF. This means that the recombination phase of the turn-OFF current phase completes sooner than that of the hotter device and the device goes into depletion faster. To maintain the overall current through the device, the lower junction temperature device depletes further to supply the mobile carriers. Since the blocking voltage is the integration of the electric field over the depletion width, the lower junction temperature IGBT consequently blocks a higher voltage since it switches faster.

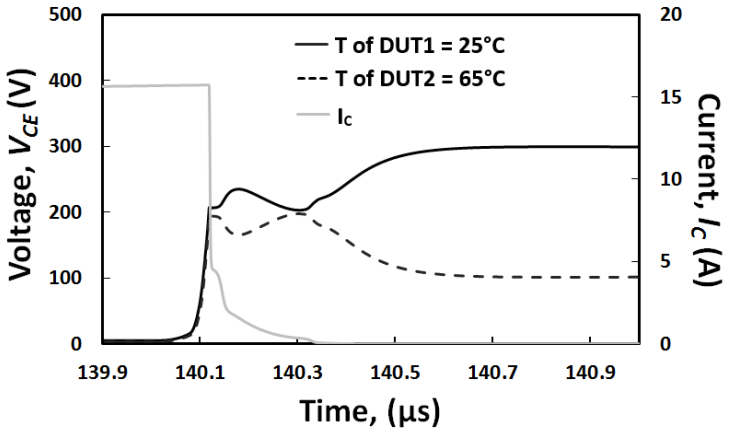


Fig. 4.17 Turn-OFF collector voltage and current in series connected silicon IGBTs with different junction temperatures

Fig. 4.18 shows the internal electric field in the fast and slow IGBTs (at 7 time instances that correspond to the labelled times t_1 to t_7 in Fig. 4.14). The internal carrier concentrations across the drift region for both IGBTs can be compared by observing Fig. 4.19 which shows the carrier concentration profiles in the drift region at times t_1 to t_7 corresponding to Fig. 4.14.

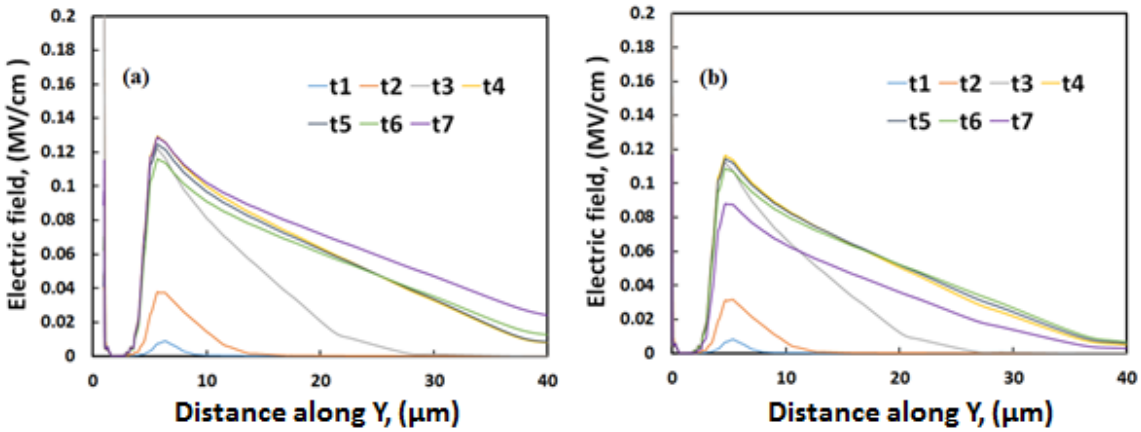


Fig. 4.18 Internal electric field in the drift region for the (a) IGBT switched with T_j=25°C (b) IGBT switched with T_j=65°C

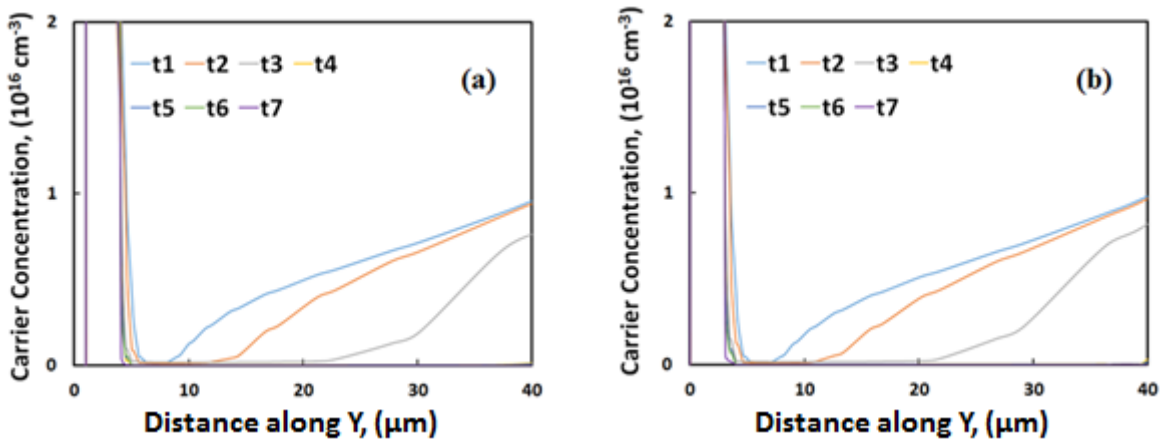


Fig. 4.19 Carrier concentration field in the drift region for the (a) IGBT switched with T_j=25°C (b) IGBT switched with T_j=65°C

Finally, simulations have been performed on series connected IGBTs with different hole carrier lifetimes. Hole carrier lifetime in IGBTs can be tailored during the fabrication according to the application requirements. For example, if the IGBT is to be used in an application with a low switching frequency and high duty ratio, like an MMC converter, then conduction losses will dominate. In this case, the hole carrier lifetime will be maximised to enable conductivity modulation of the drift region. This will mean increased switching losses, however, since the switching frequency is low then this is tolerable from the application perspective. On the other hand, if the series IGBTs are to be used in an application with a high switching frequency and smaller duty ratio, like a PWM inverter in a traction application, then switching losses are very important. In this case, the IGBT will be fabricated with low hole carrier lifetime in the drift region so that tail currents and the corresponding switching losses can be minimized. Hole carrier lifetime is controlled by defects injected in the drift region since

defects enable SRH recombination. Fig. 4.20 shows simulations of series IGBTs with a 0.1 μs and 0.5 μs carrier lifetime. As can be seen, the device with the longer carrier lifetime is unable to block any voltage since the drift region has a much higher carrier concentration rate and is therefore unable to switch as fast as the device with the short hole carrier lifetime. Fig. 4.21 shows the internal electric field in the fast and slow IGBTs (at 7 time instances that correspond to the labelled times t_1 to t_7 in Fig. 4.14). Fig. 4.22 (a) and Fig. 4.22 (b) compares the carrier concentration in the drift region for both series devices. It can be seen IGBT with the long hole lifetime never fully depletes and is consequently unable to block any voltage. The device with the short carrier lifetime then has to block all of the voltage while maintaining the series current by depleting further to supply the required current.

All of the simulations show that variations in the gate drive resistance, the junction temperature and hole carrier lifetime causes significant divergence in the turn-OFF voltage waveforms and if uncontrolled can lead to device failure if the critical field is exceeded.

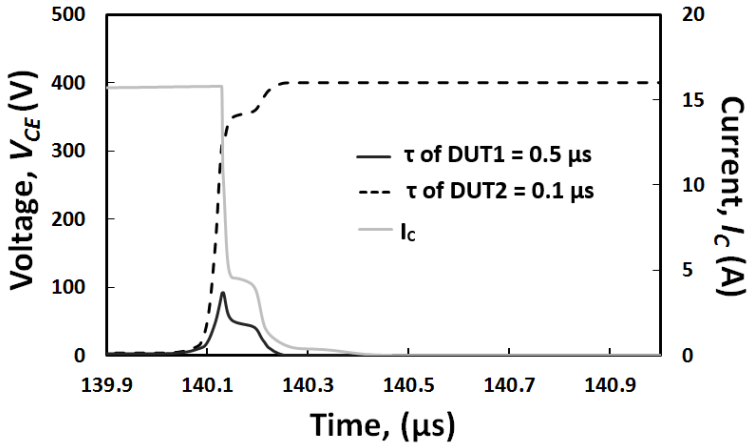


Fig. 4.20 Turn-OFF collector voltage and current in series connected silicon IGBTs with different carrier lifetimes

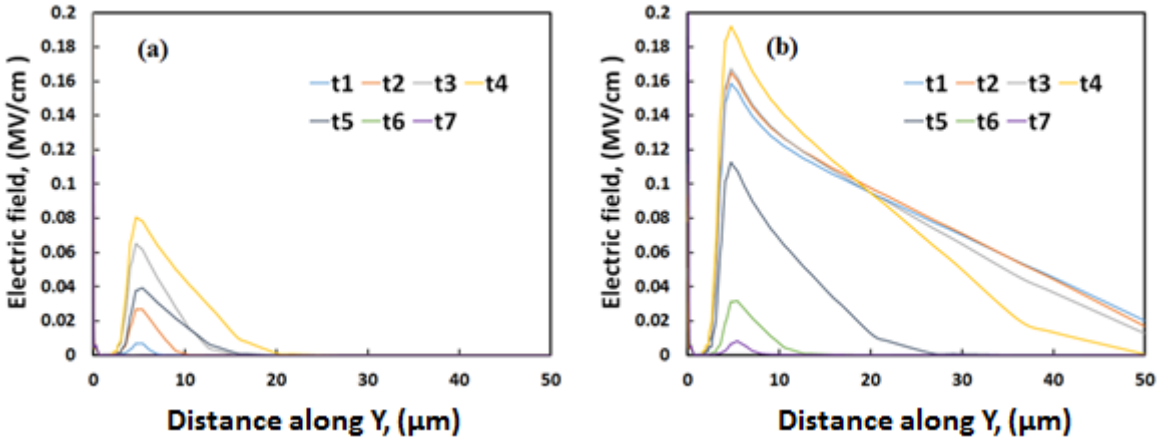


Fig. 4.21 Internal electric field in the drift region for the (a) IGBT switched with a carrier lifetime of 0.5 µs (b) IGBT switched with a carrier lifetime of 0.1 µs

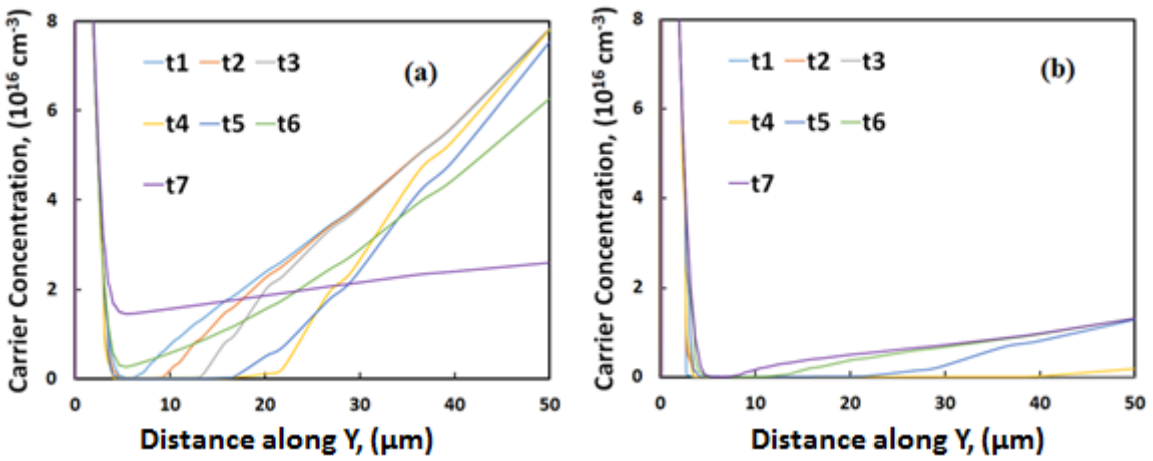


Fig. 4.22 Carrier concentration in the drift region for the (a) IGBT switched with a carrier lifetime of 0.5 µs (b) IGBT switched with a carrier lifetime of 0.1 µs

4.3.2 Finite Element Modelling of Series MOSFETs under Turn-OFF

Series connected SiC MOSFETs have been simulated in SILVACO similar to the silicon IGBTs. The parameters of the SiC MOSFETs are shown in Table 4.2 below. The clamped inductive switching performance of the series connected SiC MOSFETs have been simulated and the impact of (a) variation of the switching speed and (b) variation of the junction temperature, on dynamic voltage sharing has been investigated. Fig. 4.23 shows the transient drain voltage waveforms across each MOSFET in the series connection where one device is switched with a gate resistance of 120 Ω and the second

MOSFET is switched with a gate resistance of 100 Ω. As can be seen from Fig. 4.23 (a), the faster switching MOSFET blocks a higher drain voltage than the slower switching device. For the same variation of switching speed, compared to the silicon IGBT waveforms shown in Fig. 4.14, it can be seen that the SiC MOSFETs show less voltage divergence. The total voltage difference between the 2 series devices is 160 V for the SiC MOSFET and 360 V for the silicon IGBTs. The reason why SiC MOSFETs perform better under series connection compared to silicon IGBTs is due to the fact that the MOSFETs are unipolar devices, hence, there is no minority carrier recombination in the turn-OFF process. The turn-OFF of the power MOSFET is simply the charging of the output capacitance, hence, the capacitor that commences its charging process first will have a higher voltage across it.

Table 4.2 Details of the finite element model of the SiC MOSFET

Parameter	**Value**	**Parameter**	**Value**
Drift layer thickness (µm)	12	n^+ source doping (cm^{-3})	1×10^{20}
Drift layer doping (cm^{-3})	3×10^{15}	n^- source depth (µm)	0.8
Oxide thickness (nm)	50	p-body depth (µm)	3
p-body doping (cm^{-3})	2×10^{17}	Gate Resistance (Ω)	100
n^- drain doping (cm^{-3})	1×10^{18}	Breakdown Voltage (V)	1200
Channel length (µm)	0.8	DC Link Voltage (V)	400

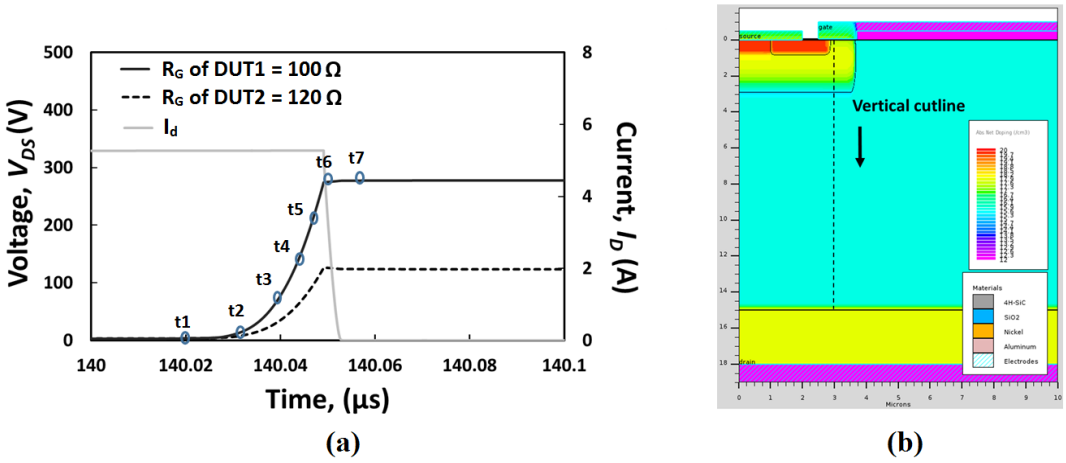


Fig. 4.23 Turn-OFF drain voltage and current in series connected SiC MOSFETs switched with different gate resistances (a) The voltage sharing between two series connected SiC MOSFETs at different switching rates; (b) SiC MOSFET cell structure cross section.

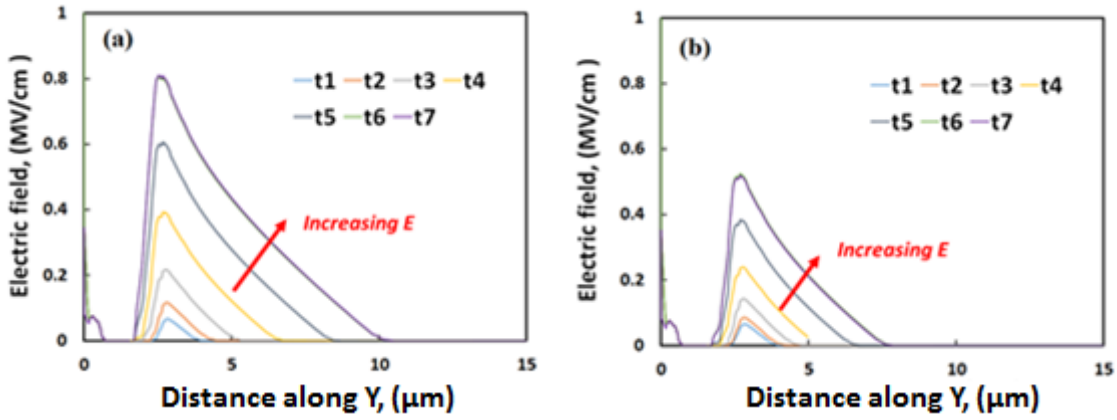


Fig. 4.24 Internal electric field in the drift region for the (a) fast SiC MOSFET (b) slow SiC MOSFET

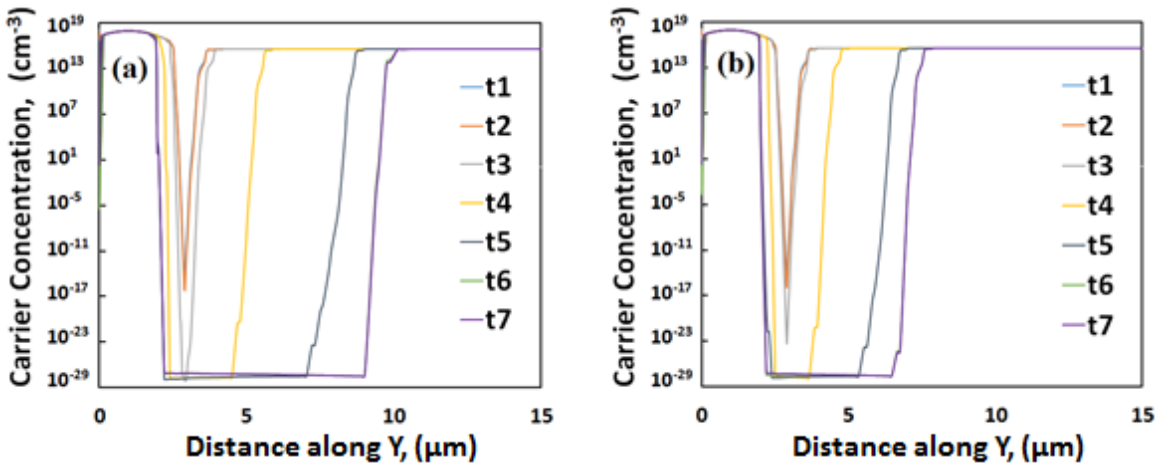


Fig. 4.25 Carrier concentration in the drift region for the (a) fast SiC MOSFET switched with 100 Ω and (b) slow SiC MOSFET switched with 120 Ω.

Fig. 4.24 (a) and Fig. 4.24 (b) shows the electric field across the voltage blocking junction of the fast and slow switching SiC MOSFET. The peak electric field occurs right at the PN junction where the depletion widths expand toward the drain junction. The electric fields have been extracted from the simulator at seven time points during the turn-OFF transient corresponding to the instances labelled t_1 to t_7 in the waveforms shown in Fig. 4.23. The faster switching SiC MOSFET has a higher peak internal electric field from time t_3 to t_7. It is also clear that the depletion width in the faster switching device extends further into the drift region than that of the slower switching device. Since the integration of the electric field over the depletion width is equal to the voltage blocked, then it follows that the faster switching device will have a higher drain source voltage than the slower switching device. At the end of the transient, the peak field in the faster switching device is approximately 0.9 MV/cm whereas it is approximately 0.6 MV/cm in the slower switching device. Series connected MOSFETs

during turn-OFF can be viewed as 2 series connected capacitors that will share voltage according to the voltage divider rule. Since the capacitors are depletion capacitances, the equation can be derived as that ratio of the permittivity (ε) of the semiconductor to the depletion width (W), which is determined by the spreading of the electric field.

$$C = \frac{\varepsilon_0 \varepsilon_r}{W} = \frac{\varepsilon_0 \varepsilon_r}{\sqrt{\frac{2q\varepsilon_0 \varepsilon_r V}{N_D}}} = \sqrt{\frac{q\varepsilon_0 \varepsilon_r N_D}{2V}} \tag{4.20}$$

It can be seen from equation (4.20) that the depletion capacitance is inversely proportional to $\sqrt{V}$. Fig. 4.25 shows the carrier concentration in the drift region extracted from the simulator along the cutline shown in Fig. 4.23 (b). By comparing the carrier concentration in the fast switching SiC MOSFET with the slow one, it can be seen that the fast switching device exhibits a more spread-out carrier concentration compared to the slow switching device. The edge of the carrier concentration profile at each time stamp in Fig.4.25 corresponds to the edge of the depletion width and the edge of the electric field shown in Fig.4.24.

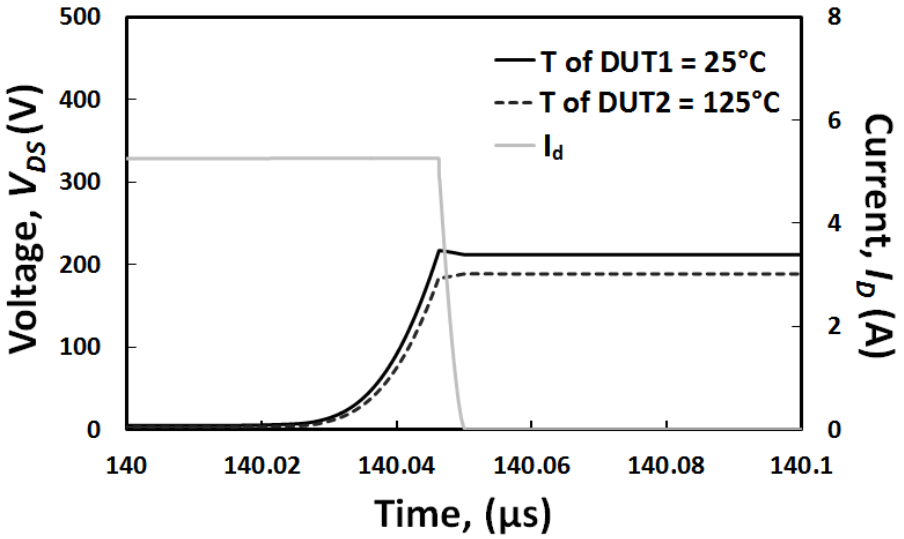


Fig. 4.26 Turn-OFF collector voltage and current in series connected SiC MOSFETs with different junction temperatures

Similar simulations of series connected SiC MOSFETs have been performed with differences in the junction temperature between the series devices. Fig. 4.26 shows the transient drain voltage waveforms across each MOSFET in the series connection where one device is switched at 25 °C and the second MOSFET is switched at 125 °C. As can be seen from Fig. 4.26 the voltage divergence is quite smaller compared to Fig. 4.23.

Fig. 4.27 shows the internal electric field in the fast and slow SiC MOSFETs (at 7 time instances that correspond to the labelled times t_1 to t_7 in Fig. 4.23). Fig. 4.28 (a) and Fig. 4.28 (b) compares the carrier concentration in the drift region for both series devices at different temperatures.

Comparing the carrier concentration profile across the MOSFET modelled in Fig. 4.25 (a) with the result shown on Fig. 4.28, at time t5 and t6, carrier concentration shows a

different behaviour. Both devices are switched with the same gate resistors, however, in results on Fig. 4.28, temperature component was enabled during the simulation. The behaviour at the abovementioned time stamps are due to carrier generation in the depletion region which increases the carrier concentration. Continuation of this generation, if it was uncontrolled and at higher temperature could lead to avalanche breakdown of the device. However, in this simulation, the device was able to dissipate the heat generated during this carrier generation in the high magnetic field in the depletion region and it successfully switched-off as shown in time stamp t7.

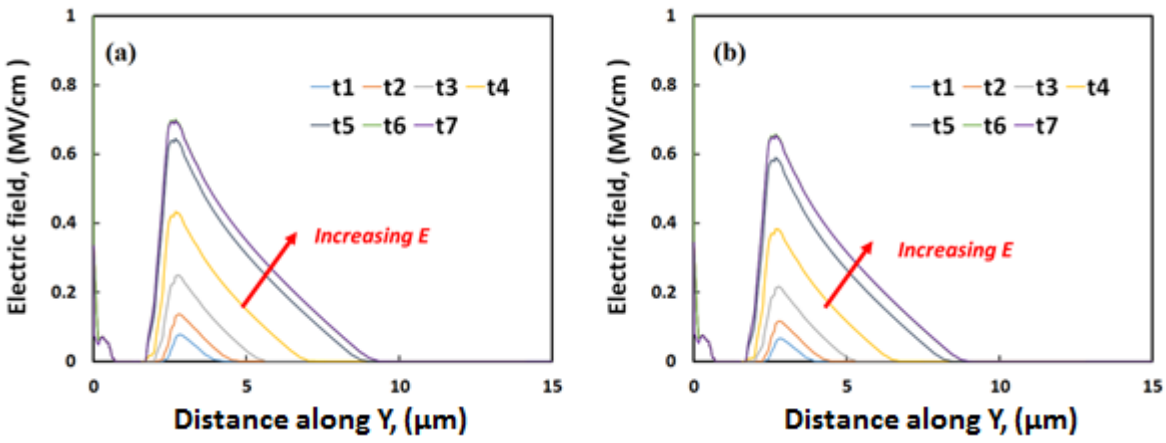


Fig. 4.27 Internal electric field in the drift region for the (a) SiC MOSFET switched with Tj=25°C (b) SiC MOSFET switched with Tj=65°C

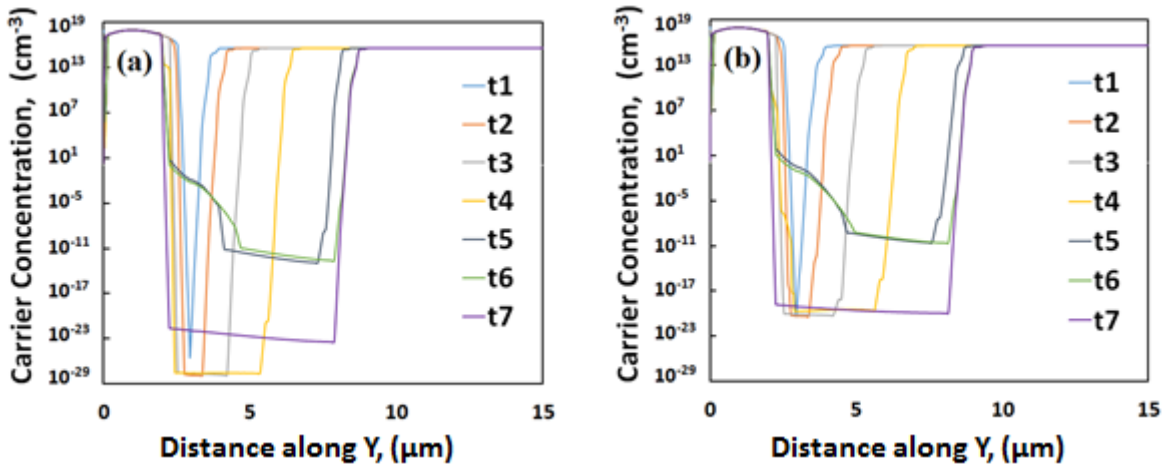
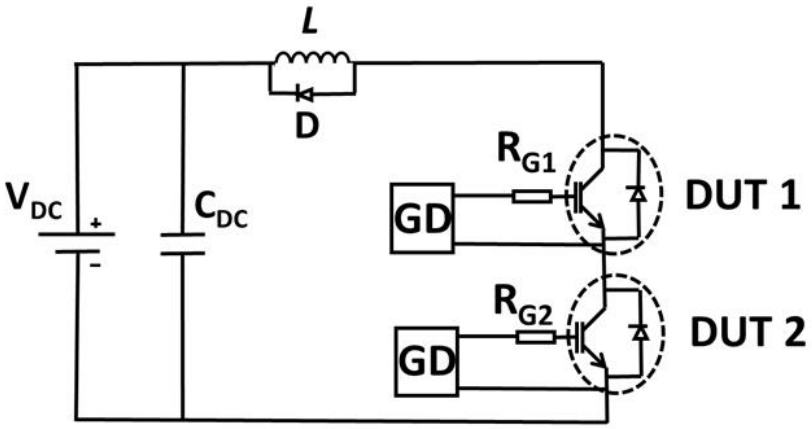


Fig. 4.28 Carrier concentration field in the drift region for the (a) IGBT switched with Tj=25°C (b) IGBT switched with Tj=65°C

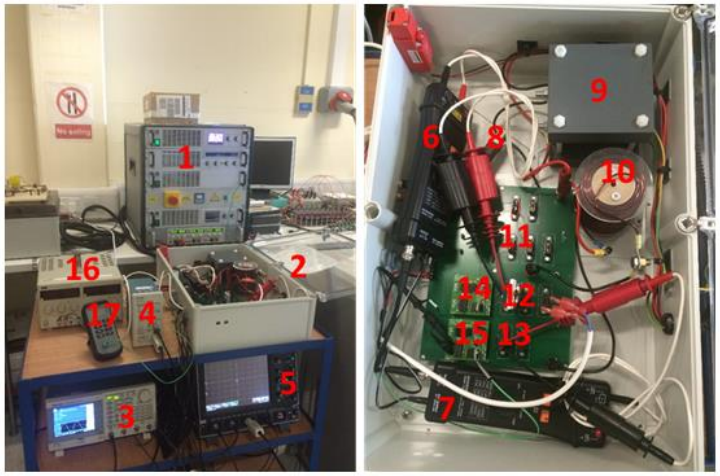
4.4 Experimental Measurements of Dynamic Voltage Sharing in Series Power Devices

A clamped inductive switching test rig that measures and characterises voltage sharing in series connected power devices has been designed and assembled. Fig. 4. shows the schematic and test rig components: (1) DC Power Supply. (2) Test Chamber. (3) Function Generator. (4) Current probe Amplifier. (5) Oscilloscope. (6) and (7) Voltage probes. (8) Current Probe. (9) DC capacitor. (10) Inductor. (11) Clamped diode (12) and (13) DUTs. (14) and (15) Gate Drives. (16) DC power supply for heater. (17) Thermometer. The test rig comprises of a 700 V power supply, a DC link capacitor, a load inductor, the devices-under-test (DUTs) and a free-wheeling diode.

As can be seen from the setup includes a 1mH inductor *L,* 490 μF dc-link capacitor C_{DC} and a 600V SiC Schottky diode with datasheet reference C3D04060E from Cree/Wolfspeed. The measurements were taken at a dc-link voltage V_{dc}=400 V, unipolar gate drive voltage V_{GG}= 0/18V and external gate resistances R_G=100/120 Ω.



(a)



(b)

Fig. 4.29 (a) Circuit schematic and (b) test rig setup

The devices under investigation are 600 V/20A Infineon Field Stop IGBTs with datasheet reference IKW20N60H3 and 650 V/39A ROHM Trench SiC power MOSFET with datasheet reference SCT3060AL.

The measurements of voltage sharing in series connected IGBTs have been performed on 600 V Field Stop IGBTs and 650V SiC Trench MOSFETs under equal temperature and switching rate conditions and with junction temperature and switching speed variation between the series pair.

4.4.1 Impact of Temperature Difference between the DUTs on Voltage Divergence during Turn-OFF

a. Si IGBTs in CIS measurements

Series connected power devices must share voltage equally in the dynamic OFF-state, however, differences in electrothermal properties may cause variation in OFF-state voltage blocking capability. The physical architecture of cooling systems in series connected power devices may cause some inevitable temperature variation between series connected power devices, hence, differences in temperature induced leakage current may cause OFF-state voltage divergence. As stated previously, series connected IGBTs, as a result of the physical architecture of the cooling system may be operating at different case and junction temperatures. This causes significant divergence in the V_{CE} characteristics of the series pair.

Fig. 4.29 shows the turn-OFF current and voltage measurements of the series connected IGBTs with both devices at different temperatures. Fig. 4.29 (a) presents the turn-OFF measurements of both devices at equal junction temperatures. During turn-OFF, there is a divergence in the V_{CE} of both IGBTs with the quicker IGBT initially blocking a higher voltage during the tail current transient.

Fig. 4.29 (b), (c) and (d) show the turn-OFF characteristics of series connected IGBTs with a junction temperature differences of 20°C, 40°C and 60°C respectively imposed by an external heater mounted to the backside of one the devices. As can be seen, the IGBT with the higher junction temperature blocks significantly less voltage with the voltage divergence between the series pair widening after the inductive over-voltage peak. The start of the voltage divergence also coincides with the commencement of the tail current in the turn-OFF characteristics of the series pair. The voltage collapse in the high temperature IGBT is due to the higher leakage current.

b. SiC MOSFETs in CIS measurements

In order to show the impact of device technology on the voltage sharing performance of series connected devices, similar measurements have been performed on series connected 650 V SiC Trench MOSFETs from ROHM. The series connected SiC trench MOSFETs were switched under clamped inductive switching conditions with both devices at equal and also under unequal junction temperature conditions. Fig. 4.30 shows the turn-OFF V_{DS} and I_D transient characteristics for series connected 650V SiC trench MOSFETs at different temperature differences.

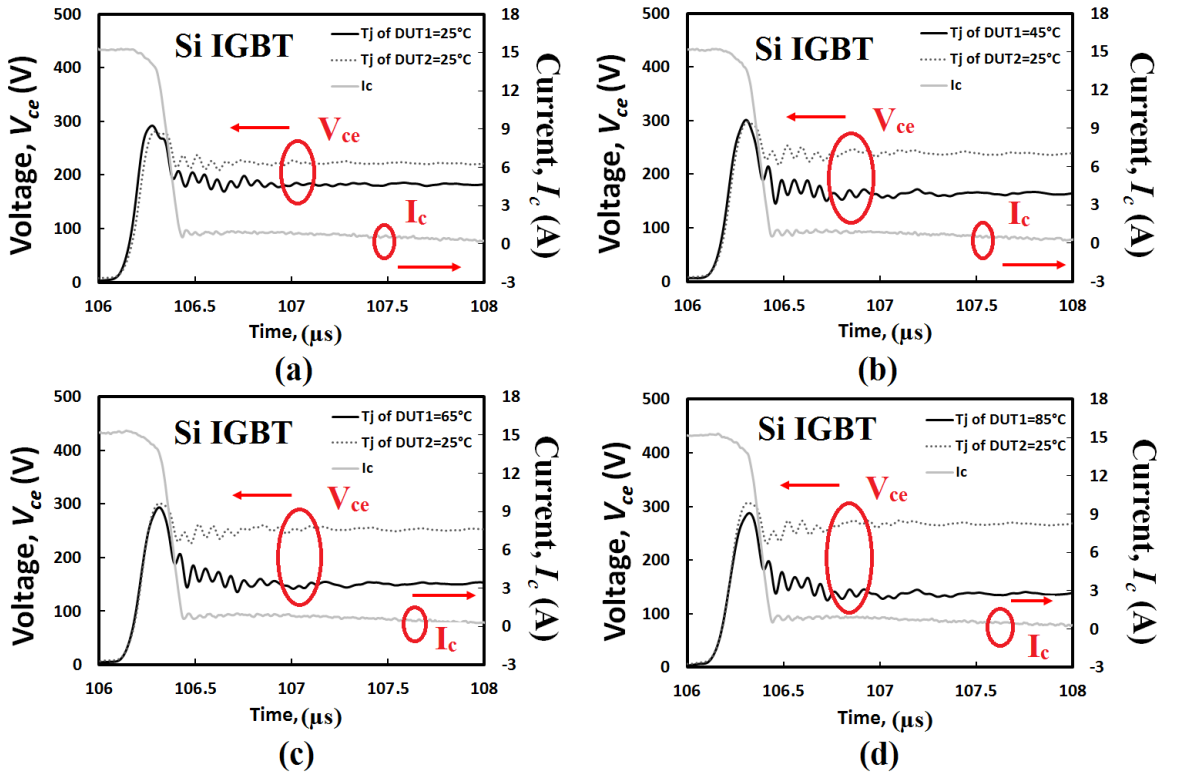


Fig. 4.29 Turn-OFF I_C and V_{CE} characteristics of series connected IGBTs under clamped inductive switching.

As shown in Fig. 4.30 (a), the measurements taken from the series connected SiC power devices at equal temperatures there is an ideal voltage sharing in the OFF state with minimal divergence in the V_{DS} characteristics. The ringing characteristics typical of SiC power devices are also evident in the turn-OFF characteristics which is mostly due to the ringing associated with the switching of the paired SiC Schottky diode on the clamped side of the circuit. Fig. 4.30 (b), (c) and (d) show the turn-OFF current and voltage transients of the series connected 650 V SiC trench MOSFETs with junction temperature mismatch of 20°C, 40°C and 60°C introduced respectively. The voltage

divergence is not as high as the silicon IGBTs. Similar to the IGBTs, the hotter device has a lower V_{DS} blocking voltage in the OFF-state.

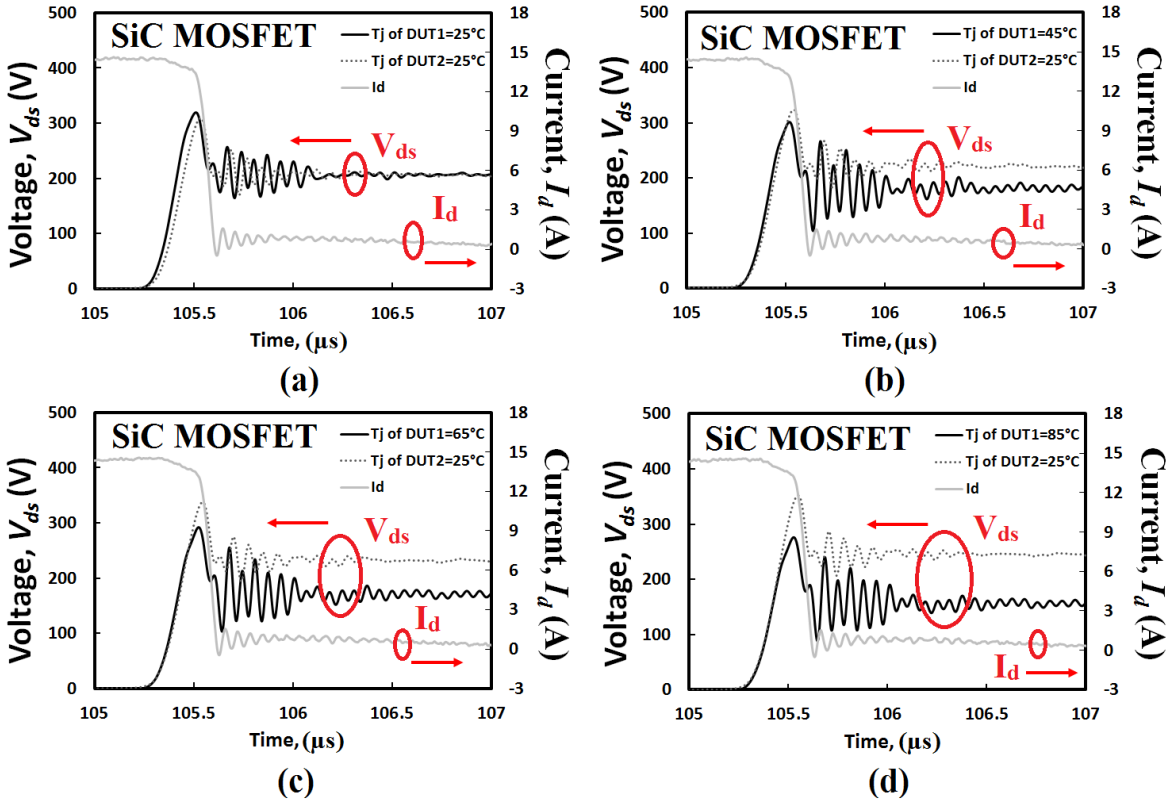


Fig. 4.30 Turn- OFF I_D and V_{DS} characteristics of series connected SiC MOSFETs under clamped inductive switching

4.4.2 Impact of Switching Rate Mismatch between the DUTs on Voltage Divergence during Turn-OFF

In order to characterize the voltage imbalance between the series connected devices, the impact of switching rate is investigated on different device technologies. As explained earlier, differences in the switching speed causes dynamic voltage imbalance

during the turn-off transient. The switching rate differences are associated with non-uniform degradation of series connected devices, non-uniform operating temperature of the devices, differences in the gate resistance due to the device layout or non-uniform gate wire-bond degradation as well as differences in the physical parameters of the device such as threshold voltage, carrier lifetime, carrier concentration and doping of the drift region. In this section, variable switching rate has been investigated for Si bipolar IGBT and the voltage balancing performance of this technology is compared with the wide bandgap SiC MOSFET devices.

The switching rate of the series connected devices is varied by changing the gate resistances. Fig. 4.31 (a) presents the turn-OFF characteristics of the series connected devices switched with the same gate resistance of R_g=100 Ohm. Fig. 4.31 (b) shows the turn-OFF current and voltage measurements of the series connected IGBTs with DUT1 switched with a smaller gate resistance (R_g=100 Ohm) than DUT2 (R_g=120 Ohm). As can be seen that the device with higher switching speed is blocking a higher voltage than the slower device which causes a big divergence in the V_{CE} characteristics.

Similar to the IGBT measurements, series connected SiC trench MOSFETs were switched under clamped inductive switching conditions with both devices under unequal switching speeds conditions to compare the voltage sharing between series connected devices of different technology. Fig. 4.33 (a) and (b) shows the turn-OFF current and voltage transients of the series connected 650 V SiC Trench MOSFETs with equal and different switching speeds. The voltage divergence is not as significant as for the silicon IGBTs. However the rate of divergence is higher than by applying

temperature mismatch. Similar to the IGBTs, the slower device has a lower V_{DS} blocking voltage in the OFF-state.

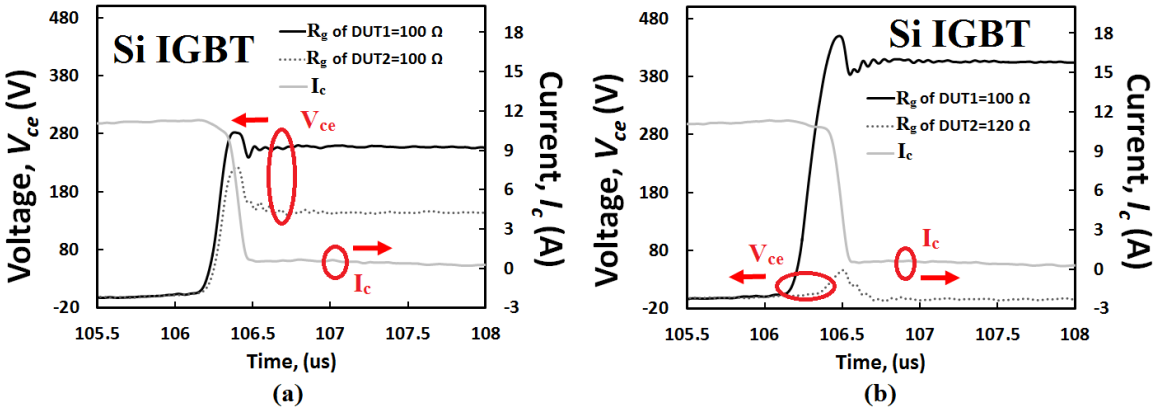


Fig. 4.31 Turn- OFF I_{CE} and V_{CE} characteristics of series connected IGBTs under clamped inductive switching with different switching rates between IGBTs.

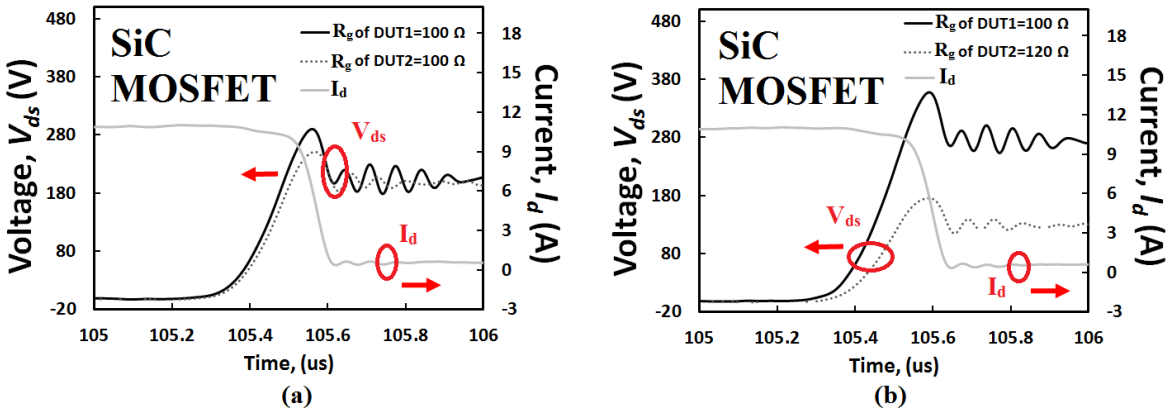


Fig. 4.32 Turn- OFF I_{DS} and V_{DS} characteristics of series connected SiC MOSFETs under clamped inductive switching with different switching rates.

4.5 Conclusion

In this chapter, the switching transient behaviour of series connected IGBT and SiC MOSFETs during Turn-OFF was investigated at different operating conditions (temperature and switching rate) and compared the two technologies through experimental results justified by finite element models as well as compact Matlab/Simulink models. Using the FEM of Si IGBT and SiC MOSFET power devices, the transients of voltage sharing were compared under unbalance switching rate and it was discussed that the voltage imbalance for Si IGBT is highly dependent on the carrier concentration in the drift region during switching while for SiC MOSFET it depends on the switching time constant of the gate voltage and the rate that the MOS-channel cuts the current. It was shown that SiC MOSFET shows a better performance during the OFF-state and switching transients in comparison to the conventional Si IGBTs.

4.6 References

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Chapter

5 Series Connected Devices Under Dynamic Avalanche Conditions

5.1 Introduction

As power devices are series connected for voltage sharing, loss of gate drive synchronization and/or variation in device switching time constant can cause voltage imbalance between the series devices. This voltage imbalance can have destructive consequences if uncontrolled as it takes the device into avalanche mode conduction is the critical field of the semiconductor is exceeded. Capacitors (in snubbers) are usually designed in to maintain series voltage balance under dynamic conditions [1], however, in snubberless designs, where active gate drivers are used for voltage balancing during switching transients [2], it is necessary to evaluate the limits of the power device under transient unsynchronized switching [3-6, 22-25]. This is important for defining the resolution and bandwidth of the active gate controller system since its purpose is to control voltage divergence between the series devices. Desynchronization of the gate

drivers in series connected devices will cause the faster switching device into avalanche during turn-OFF and the slower device into avalanche during turn-ON. Power device failure from BJT latch-up in MOSFETs and thyristor latch-up in IGBTs can result in potentially destructive consequences for the entire converter [7-8, 15]. As one device in the series chain fails, failure in other devices is accelerated since the remaining voltage has to be shared within fewer devices thereby increasing the electric fields. Failure of the power device under avalanche is exacerbated by the (i) high device commutation rates (ii) device junction temperature (iii) increasing magnitude of gate drive switching mismatch and (iv) high ratio of the DC bus voltage to intrinsic breakdown voltage of the device. Using experimental measurements of series connected power devices and finite element simulations in SILVACO, this chapter investigates the performance of series connected SiC power MOSFETs and silicon IGBTs under dynamic avalanche conditions. By introducing delays between the gate drivers at different switching speeds and different DC link voltages, correlations have been established between the maximum gate trigger mismatch (between the series pair) and electrothermal failure under dynamic avalanche. This information is important for power electronics engineers designing active gate controllers for series connected power devices because it defines the boundary conditions for the bandwidth of the controllers. By simulating and measuring the limits of the power devices under dynamic avalanche as a function of the switching speed and the operational voltage, it is possible of develop a design methodology for optimising compactness, switching loss performance and avalanche ruggedness of the converter.

5.2 Avalanche mode conduction and latch-up of Power Devices

This chapter of the thesis focuses on the performance of series connected SiC power MOSFETs and silicon IGBTs under dynamic avalanche conditions that result from a loss of gate synchronization. Power transistors can conduct current under avalanche mode conditions when the normal means of current conduction (drift and diffusion) mechanisms are not in place. This is not a normal mode of conduction since the device is usually not ON under such conditions. Power MOSFETs conduct current via the drift of majority carriers through a channel which is controlled by a gate voltage. IGBTs have the added mechanism of hole injection from the p-type collector to enable conductivity modulation via recombination with electrons injected from the MOS channel. Under avalanche mode conduction, carrier flow is due to the uncontrolled generation of electron-hole pairs which occurs during impact ionisation. Under this condition, the channel is OFF and the electron-hole pairs are generated by carriers flowing under the influence of a high electric field across the device. If the field is high enough, meaning that there is significant depletion across the voltage dropping PN junction, then mobile electrons are accelerated by the electric field and gain sufficient kinetic energy. If the kinetic energy is greater than the energy bandgap of the device, then electron-hole pairs will be generated when collision occurs between the free electrons and the crystal lattice. The newly generated electrons repeat this process until sufficient carriers are generated to conduct current in the OFF-state. The electric field at which this occurs is called the “critical electric field” and is higher for SiC than

silicon. This is because the wider bandgap in SiC means that more energy is needed by the moving stray electrons to generate additional electron-hole pairs.

Avalanche mode conduction can occur when the device is forced to conduct current when the gate voltage is OFF. The absence of the channel forces the device into avalanche mode conduction. This is usually referred to as unclamped inductive switching (UIS) or static avalanche [9, 12, 13, 29]. Avalanche mode conduction can also occur under dynamic conditions during switching. This occurs more for IGBTs when the uncompensated hole current that results from an abrupt supply of electron current triggers the parasitic thyristor that is soon to be discussed. Avalanche mode conduction can also occur in the event that the voltage across the power device exceeds the breakdown voltage of the device. This can happen if excessively high current commutation rates coupled with parasitic inductances in the path of current flow cause excessive voltage overshoots across the device [10, 11]. This can also happen under conditions of extreme voltage imbalance in series connected devices.

When power devices under avalanche mode conduction, the magnitude of the current and the duration of the avalanche conduction interval will determine if the power device can withstand the energy dissipated. During avalanche mode conduction, the drain-source voltage of the MOSFET (or collector-emitter voltage of the IGBT), is at its intrinsic value meaning that there is significantly higher instantaneous power dissipation across the power device compared to the power generated from conduction or switching losses. Power MOSFETs contain parasitic BJTs whereas power IGBTs contain parasitic thyristors. If these parasitic components

turn-ON, or latch during avalanche mode conduction, then thermal runaway may occur thereby causing potentially destructive electro-thermal failure [11-14]. During thermal runaway, there is significant temperature inequality across the chip, hence current crowding results in thermal destruction.

Fig. 5.1 shows the equivalent circuit of a power MOSFET (that contains the parasitic BJT) during normal mode conduction while Fig. 5.1(b) shows the MOSFET equivalent circuit during avalanche mode conduction. As can be seen, during avalanche mode conduction, current is conducted through the parasitic BJT. As can be seen from Fig. 5.1 (a), the emitter of the parasitic BJT coincides with the physical source of the MOSFET, while the collector of the parasitic BJT coincides with the physical drain of the MOSFET. The gate of the BJT coincides with the body of the MOSFET. From elementary theory of PN junctions, a BJT turns ON when the emitter-base junction is forward biased and the base-collector junction is reverse biased. Hence, for the parasitic BJT to latch, there must be source-to-body voltage within the power MOSFET that is non-zero [12, 16]. Device manufacturers try to suppress this from occurring by ensuring that the source is sufficiently grounded to the body thereby eliminating the possibility of a floating body or a forward biased source-body PN junction i.e. the body voltage becomes greater than the source voltage. This is done by using what is called a deep p-body implant that ensures a low resistance contact between the source and the body. However, under high temperature conditions, the resistivity of this implanted region increases as a result of increased phonon scattering thereby increasing the possibility of a forward biased source-body PN junction.

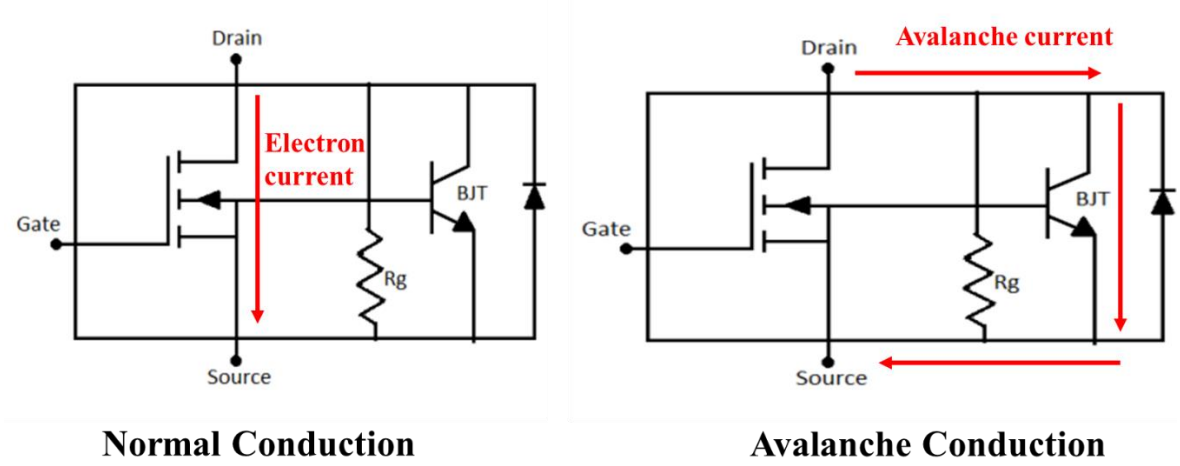


Fig. 5.1 (a) MOSFET equivalent circuit showing parasitic BJT and normal conduction current path (b) Current path during avalanche mode conduction

Parasitic thyristor latch-up can also occur in IGBTs. Fig. 5.2 shows the equivalent circuit of an IGBT including the parasitic thyristor with the current flowing through normal drift-diffusion mechanisms. Included in the equivalent circuit are the lumped drift resistance of the voltage blocking region and the p-body resistance of the MOS channel. The drift resistance depends on the thickness of the voltage blocking drift region, the doping of the region as well as the minority carrier lifetimes during ON-state. In this case, since the IGBT is a bipolar device, electron current flow occurs through the channel of the IGBT from the emitter into the p-body while hole current flows from the collector of the IGBT into the drift region. Conductivity modulation occurs in the voltage blocking drift region when electrons and holes recombine with electrons coming from the channel and holes coming from the forward biased PN junction at the collector. This process of conductivity modulation is what makes IGBT

more suitable for higher voltage applications over MOSFETs since the conduction losses are minimized. Fig. 5.2 (b) shows the equivalent circuit of the IGBT under avalanche mode conduction. When the device is turned-OFF, the supply of electrons from the MOS gate is abruptly ended. As a result, the hole current is uncompensated thereby resulting in a large diffusion of holes across the body of the IGBT. The hole current flows through the p-body resistance resulting in a voltage drop across that resistance. If that voltage is sufficient to activate the parasitic thyristor by turning ON the parasitic NPN BJT, then destructive failure can occur similar to BJT latch-up in power MOSFETs. For the thyristor to latch, the sum of the gains of the NPN and PNP BJTs must be equal to or greater than 1 [12, 17-19]. To supress this effect, device manufacturers insert additional low resistivity p-body implants in an effort to prevent the NPN BJT from latching.

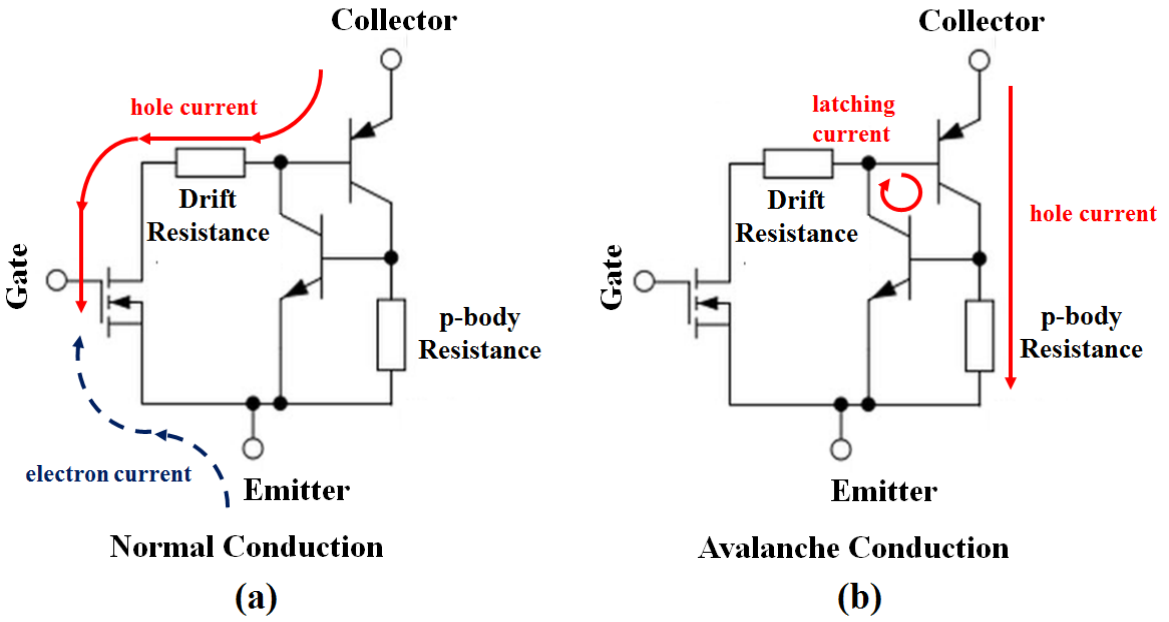


Fig. 5.2 (a) IGBT equivalent circuit showing parasitic thyristor and normal conduction current path (b) Current path during avalanche mode conduction.

Series connected devices need to be synchronised during turn-ON and turn-OFF, otherwise individual devices may exceed their voltage rating if the OFF-state voltage is not properly distributed. Loss of synchronisation can result from (i) gate misfiring signals (ii) differences in device commutation rates (iii) differences in device junction temperature and (iv) variations in other electrical parameters including minority carrier lifetime, input capacitance, threshold voltage etc. Snubbers are typically used to ensure static and dynamic voltage balancing. In the OFF-state, the resistors in the snubbers ensure that the leakage currents are under control and do not contribute to uncontrolled OFF-state voltage divergence. Under dynamic conditions, the capacitors in the snubbers ensure that the voltage balance is maintained. An example of a commercial converter that uses series connected devices is the IXYS 10kV/1kA 3L-NPC

voltage source converter that uses series connected press-pack IGBTs and PiN diodes [20]. Fig. 5.3 shows a phase leg of the converter where an RCD snubber can be seen connected across each device in the converter. Also shown in the figure is the picture of the series stacked IGBTs and PiN diodes. The size and losses caused by the snubber has motivated researchers to investigate means of ensuring controlled voltage control using active gate drivers [33]. However, if active gate drivers are to be implemented in future converters using series connected devices, a detailed characterisation of the ruggedness performance of the series connected devices is necessary. This is what this chapter is dedicated to.

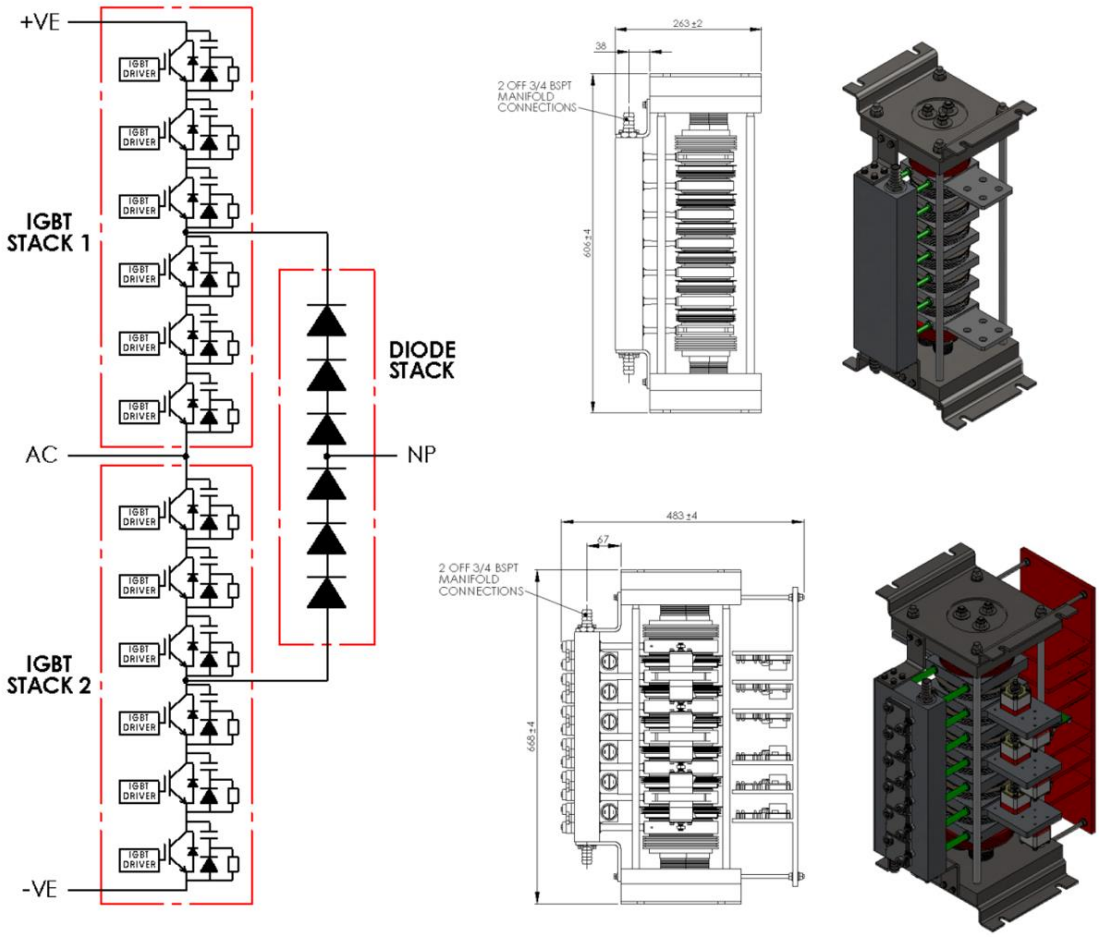


Fig. 5.3 IXYS 3-L 10kV/1kA NPC Voltage Source Converter based on Series Stacked Press-pack IGBTs and Diodes [19]

When series connecting power devices for voltage sharing in the OFF-state, there are a number of considerations that impact on the overall size (complexity), losses and ruggedness under avalanche conditions. Power devices are usually designed with significant safety factor regarding voltage use, hence, a device that is rated at 1.2 kV will typically have an intrinsic breakdown voltage of 1.5kV to 2 kV. In SiC power MOSFETs, these margins are noticeably higher compared to IGBT perhaps to

accommodate the very high voltage overshoots that result from high current commutation rates [8, 21]. When designing converters that use series connected devices, the following considerations will come into play

i) **The ratio of the operational voltage to the device intrinsic breakdown voltage:** The operational voltage will be determined by the ratio of the total DC link voltage to the number of series connected devices. Hence, if the DC link voltage is V_{DC} and there are N devices, then the operational voltage will be given by

$$V_{op} = \frac{V_{DC}}{N} \tag{5.1}$$

Clearly, if there are more devices in the series link, then the operational voltage of each device is reduced. This means that the devices are less prone to failure under dynamic avalanche is there is gate misfiring due to the increased headroom between the operational voltage and the intrinsic breakdown voltage [30]. However, the system is more expensive. Reducing the number of series devices reduces the cost of the system, however, at the expense of making the converter less rugged under dynamic avalanche conditions. In this case, there is less margin for error in the performance of the active gate driver.

ii) **Commutation rate of the Power Devices:** The commutation rate is set by the electrical time constant which depends on the total gate resistance and the input gate capacitance. The total gate resistance is the sum of the internal and external gate resistance. The internal gate resistance depends on the

internal mask layout of the transistor and is given as an immutable property of the device. The external gate resistor can be changed and is therefore a design parameter. The input capacitance of the device is the sum of the gate capacitance and the Miller capacitance. When series connected devices are driven with high commutation rates, by using a small external gate resistance, drain-source (or collector-emitter) voltage overshoots result from the product between the current commutation rate the parasitic inductance in the path of the current flow. As the switching rate is increased, the peak voltage at turn-OFF may exceed the intrinsic breakdown voltage of the device thereby taking the device into dynamic avalanche with potentially destructive consequences. This is more so the case in series connected devices that are not properly synchronised. Using high switching rates will reduce the switching losses however, at the expense of making the converter less rugged under dynamic avalanche conditions due to loss of series device gate synchronization. Using low switching rates will increase the switching losses however, with the benefit of reducing peak overshoots and increasing the ruggedness of the system under dynamic avalanche conditions.

iii) **Accuracy and Bandwidth of the Active Gate Controller:** The active gate controller is charged with the responsibility of intelligently driving the series power devices while controlling voltage divergence between them. To do this, the controller is fed from voltage sensors that measure the voltage across the device and adjusts the gate voltages of the power devices while driving them

in linear mode. The output voltage of the device is most sensitive around the plateau voltage region of the gate characteristic due to the fact that the Miller capacitance is responsible for the output voltage transient. By increasing the gate voltage, the output voltage is reduced likewise reducing the gate voltage increases the output voltage. The sampling speed and bandwidth of the control process is important to ensure that voltage divergence is kept under control since uncontrolled voltage divergence may cause damage before remedial action is taken if the bandwidth of the controller does not keep up with the rate of voltage divergence [22-25].

There are trade-offs when considering the three factors discussed above in regard to designing systems that use series connected power devices. For example, if the operational voltage and the switching rate is maximised, the error margin of the active gate controller is very small since the conditions for dynamic avalanching are more acute. Slight mismatches in gate propagation delay between the series devices can cause device failure under dynamic avalanche. The converter may be more compact with reduced losses however, a high bandwidth controller is needed. On the other hand, if the operational voltage and the switching rate is reduced, then the converter is able to tolerate larger magnitudes of gate mismatch (because of the greater voltage headroom) however, this is at the expense of increased losses and more complexity. It should be noted that the switching rate and operational voltage can be traded off against one another depending on the priority of the designer. If switching losses are a

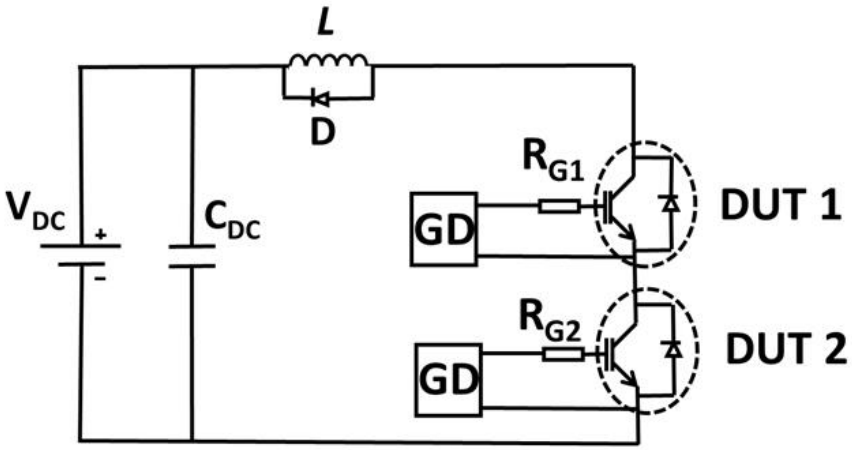
paramount consideration, then the switching rate can be maximised and the operational voltage reduced.

5.3 Experimental Set-up for Dynamic Avalanche Performance

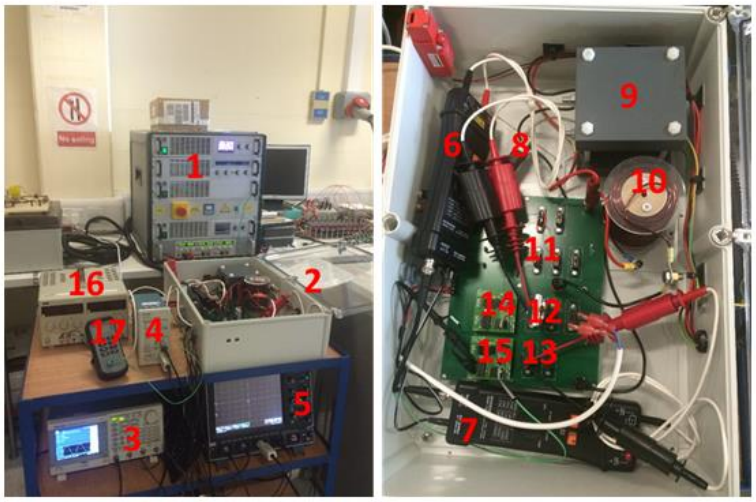
This To investigate the impact of unsynchronized switching between series connected devices for different technologies a test rig was designed and experiments were carried out to characterize the performance of series connected power devices. The circuit schematic and the experimental setup for characterizing the turn-OFF transient of power devices are shown in Fig. 5.4 (a) and (b) respectively. The test-rig setup includes: (1) DC Power Supply. (2) Test Chamber. (3) Function Generator. (4) Current probe Amplifier. (5) Oscilloscope. (6) and (7) Voltage probes. (8) Current Probe. (9) DC capacitor. (10) Inductor. (11) Clamped diode (12) and (13) DUTs. (14) and (15) Gate Drives. The devices under investigation were 600 V/20A Infineon Field Stop IGBTs with datasheet reference IKW20N60H3 and 650 V/39A ROHM SiC trench power MOSFET with datasheet reference SCT3060AL. A 1200V/16A SiC Schottky diode with datasheet reference IDH16G120C5 was used as the clamping diode.

The DC link voltage of the power devices was originally set so that each device would block half its rated voltage. To determine the SOA of the power devices under dynamic conditions, a mismatch is introduced into the gate driver signals, thereby

causing the devices to switch at different instances. The mismatch is in the form of a gate signal delay between the 2 gate drivers. The magnitude of this gate activation delay is varied together with the device current/voltage commutation rate which is controlled by the gate resistance. Hence, for a given gate resistance, the gate signal delay between the gates of the series connected devices is varied until the device exceeds the SOA thereby going into avalanche and potentially destructive latch-up. For gate signal delay between 2 series connected devices, the faster switching device may go into avalanche during turn-OFF and the slower switching device may go into avalanche during turn-ON. The SOA under these conditions depend on (i) the magnitude of gate signal delay (ii) the magnitude of the inductive voltage overshoot during turn-OFF and (iii) the ratio of the measured peak voltage to the rated voltage.



(a)



(b)

Fig. 5.4 (a) Circuit schematic and (b) test rig setup.

5.4 Experimental Measurements and Results

Fig. 5.5 (a), (b) and (c) show the turn-OFF voltage and current waveforms of series connected IGBTs. Fig. 5.5 (a) shows the case where the gate drivers are perfectly synchronized. It can be seen from Fig. 5.5 (a) that the devices share the total voltage equally. As the delay between the gate trigger signals of the two series connected devices increase, the faster device starts blocking higher voltage than the other device. Fig. 5.5 (b) shows the turn-OFF transient waveforms of the series connected IGBTs with 233 ns gate delay. It can be seen from Fig. 5.5 (b) that the faster switching IGBT blocks the DC link voltage entirely. This is the maximum delay that could be applied to the gate of the device before the failure of the device would happen. A further delay between the switching of the two devices would lead to avalanche breakdown of the faster device. In this pre-failure mode, the faster device enters a dynamic avalanche in which, the collector-emitter voltage of the device shows a slower ramp rate followed by a momentary rise of the voltage to the breakdown voltage of the device. As can be seen, the dV/dt of the device starts-off with a ramp rate which is dependent on the charging rate of the fixed gate-oxide capacitance of the device coupled with the gate resistance. The second ramp rate is voltage dependent and is due to the charging of the Miller capacitance of the device. This slope is fixed by the dynamic avalanche process. Fig. 5.5 (c) shows the measurements for a case where there is a 240ns delay between the gate

drivers. It can be seen from Fig. 5.5 (c) that the fast switching device, DUT1, goes into destructive failure since the maximum blocking voltage has been exceeded. At approximately 600ns, DUT1 (the faster IGBT) fails through thyristor latch-up and thus results in a short circuit. At that instant, the current, which was initially commutating into the free-wheeling diode, starts to rise through the IGBT as can be seen between 600 ns and 900 ns in Fig. 5.5 (c).

The measurements of the series connected IGBTs have been repeated over a wide range of switching rates by using different gate resistances. It was observed that increasing the switching rate reduces the magnitude of the gate delay required for thyristor latching and destructive failure. This is because the peak inductive voltage overshoot during turn-OFF increases with the switching rate, hence, the potential for latching and destructive failure increases concomitantly. Fig. 5.6 shows picture of the IGBTs after package removal a) normal IGBT b) failed IGBT under dynamic avalanche breakdown, whereas Fig. 5.7 presents the microscopic picture of the chip of same IGBTs respectively.

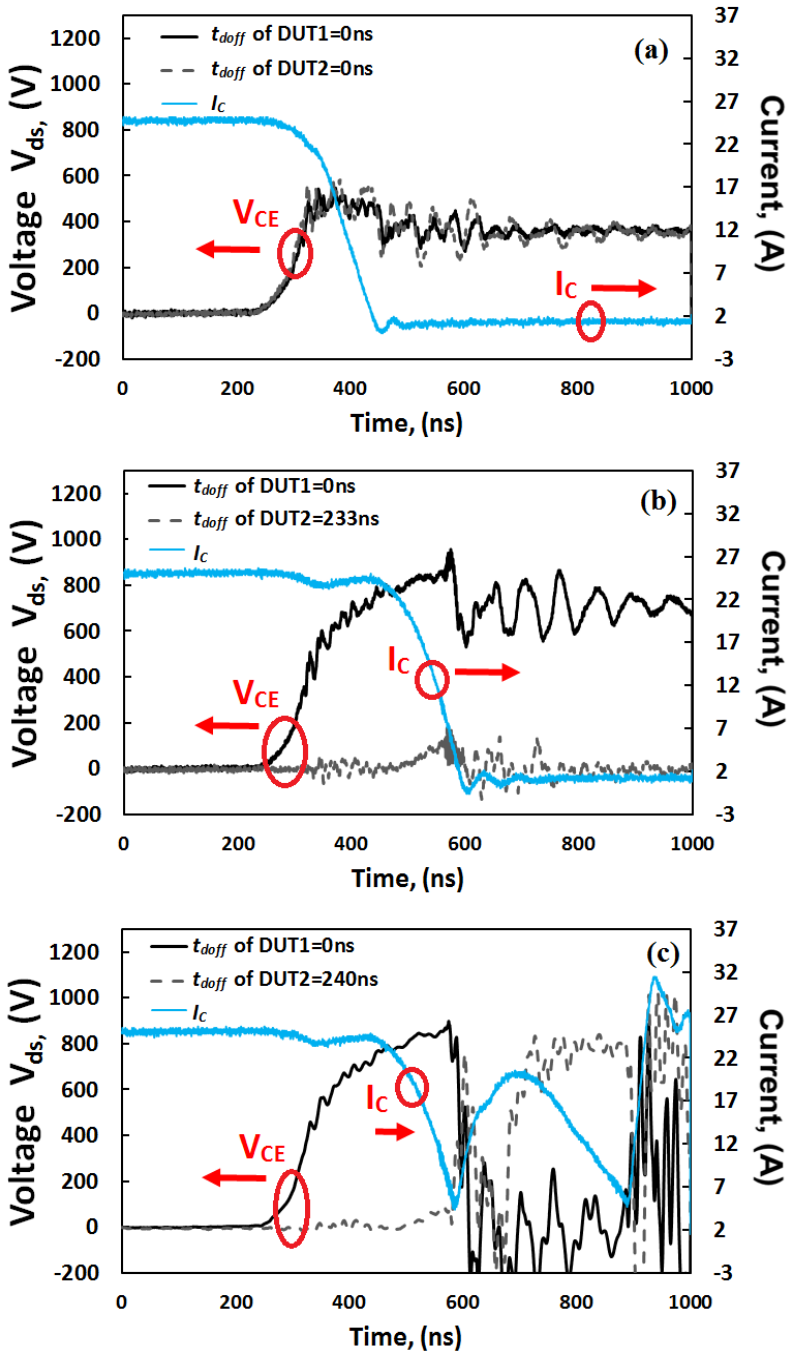


Fig. 5.5 Current and Voltage waveforms of series connected silicon IGBTs during turn-OFF with (a) perfectly synchronized gates (b) 233ns gate delay pre-avalanche condition and (c) 240 ns gate delay leading to avalanche breakdown.

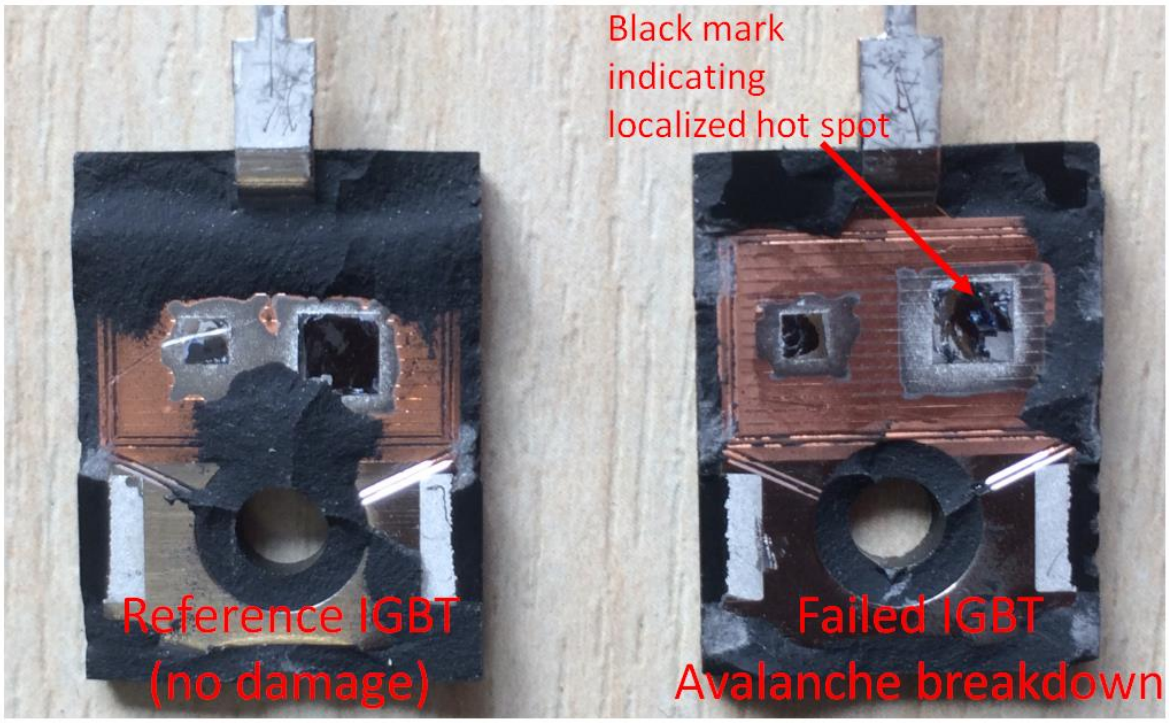


Fig. 5.6 Picture of Si IGBTs after package removal: reference IGBT with no damage and failed IGBT due to avalanche breakdown.

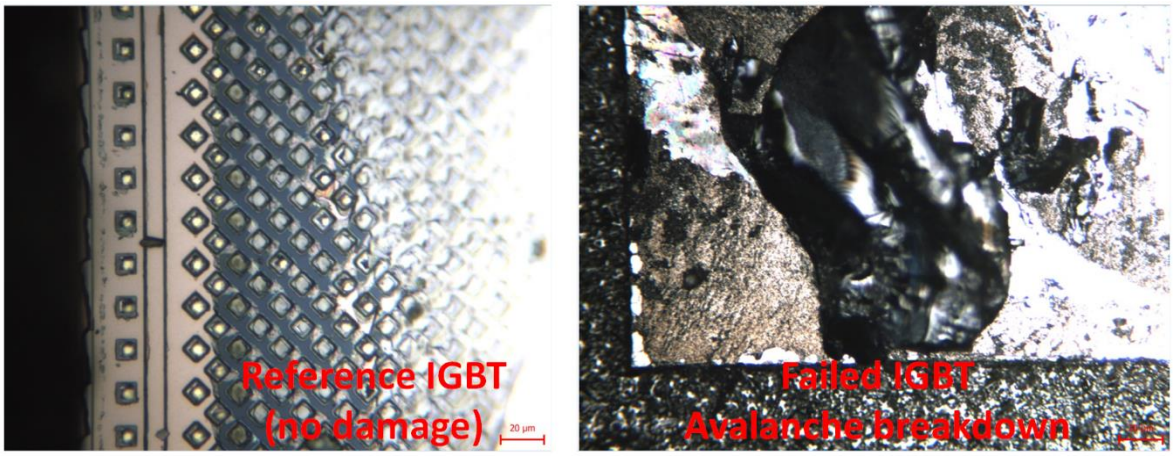


Fig. 5.7 Microscopic picture of the IGBT chip after package removal.

The measurements of the turn-OFF transient for series connected IGBTs that were done for several switching rates is shown in Fig. 5.8 (a) for a DC link voltage of 650V

and (b) for a DC link voltage of 700V. Figure 5.8 shows the ratio of the peak measured voltage to the breakdown voltage of the device as a function of switching rate and the maximum gate mismatch delay before failure under latch-up. In both Fig. 5.8 (a) and Fig. 5.8 (b), the shaded regions on the plots indicate measurement points where destructive failure through thyristor latching occurred. Hence, the SOA of the series pair is clearly identified in both plots. The general trends show that the SOA reduces as the DC link voltage is increased and that there is a trade-off between the need to increase the switching rate (to reduce switching losses) and the maximum allowable delay in gate signaling between the series pair. The SOA reduces with increasing DC link voltage and increasing switching rate. The SOA plots can be very useful for converter design engineers that need to know the limits of the gate signaling delay in active gate drive systems.

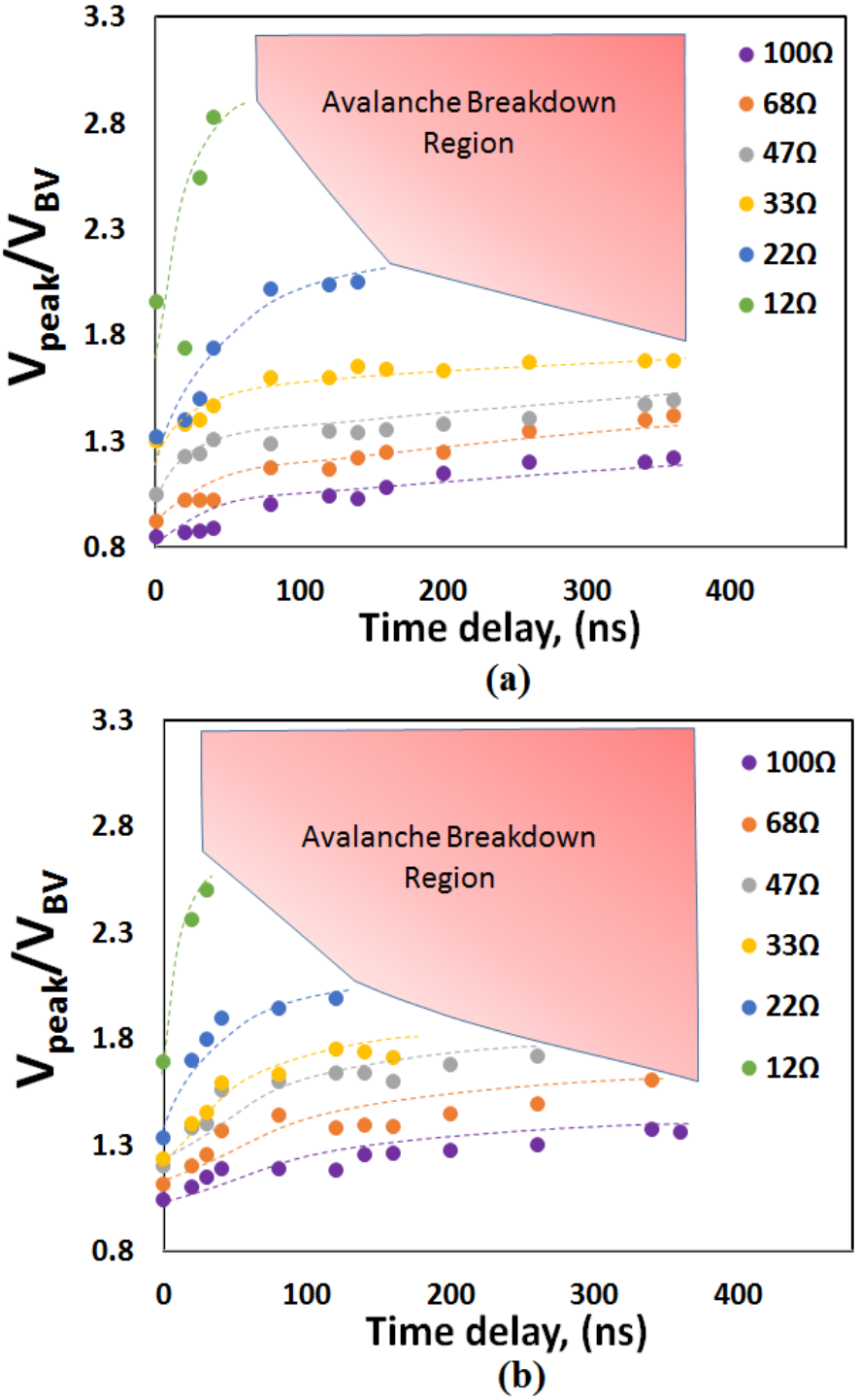


Fig. 5.8 Ratio peak measured voltage to rated breakdown voltage of Si IGBT as a function of the gate signalling delay. (a) 650V (b) 700V.

Similar measurements have been done on SiC MOSFETs. The gate signaling delay was varied over a wide range for series connected 650V SiC trench MOSFETs at 700V DC link voltage. The turn-OFF transient voltage and current waveforms for the series devices are shown in Fig. 5.9 (a) for perfectly timed gate signals and Fig. 5.9 (b) for a maximum delay of 240 ns. Unlike the silicon IGBTs, the SiC devices did not undergo avalanche failure. SiC MOSFETs are known to be more avalanche capable as various investigations have shown that the devices can dissipate larger amounts of avalanche energy without latch-up. Although the switching rates are higher (hence the turn-OFF voltage waveforms are prone to have higher inductive voltage overshoots) the larger headroom in the blocking voltage is critical in ensuring the SiC MOSFETs do not undergo avalanche during desynchronized turn-OFF of series connected devices. It also important to note that temperature imbalance between the series devices can become critical since the switching rates in SiC are known to be temperature sensitive [26, 27].

Fig. 5.10 shows the turn-OFF current waveforms with different magnitudes of gate mismatch delay for the series Silicon IGBT in Fig. 5.10 (a) and the series SiC trench MOSFET in Fig. 5.10 (b). The rightward shift of the current waveform is due to increasing gate mismatch delay. It can be seen that the turn-OFF current waveform shifts rightwards in time and for the silicon IGBT, the current rises uncontrollably during turn-OFF for the longest gate signaling delay (240 ns). The sudden rise of current at 600 ns is due to the IGBT latch-up.

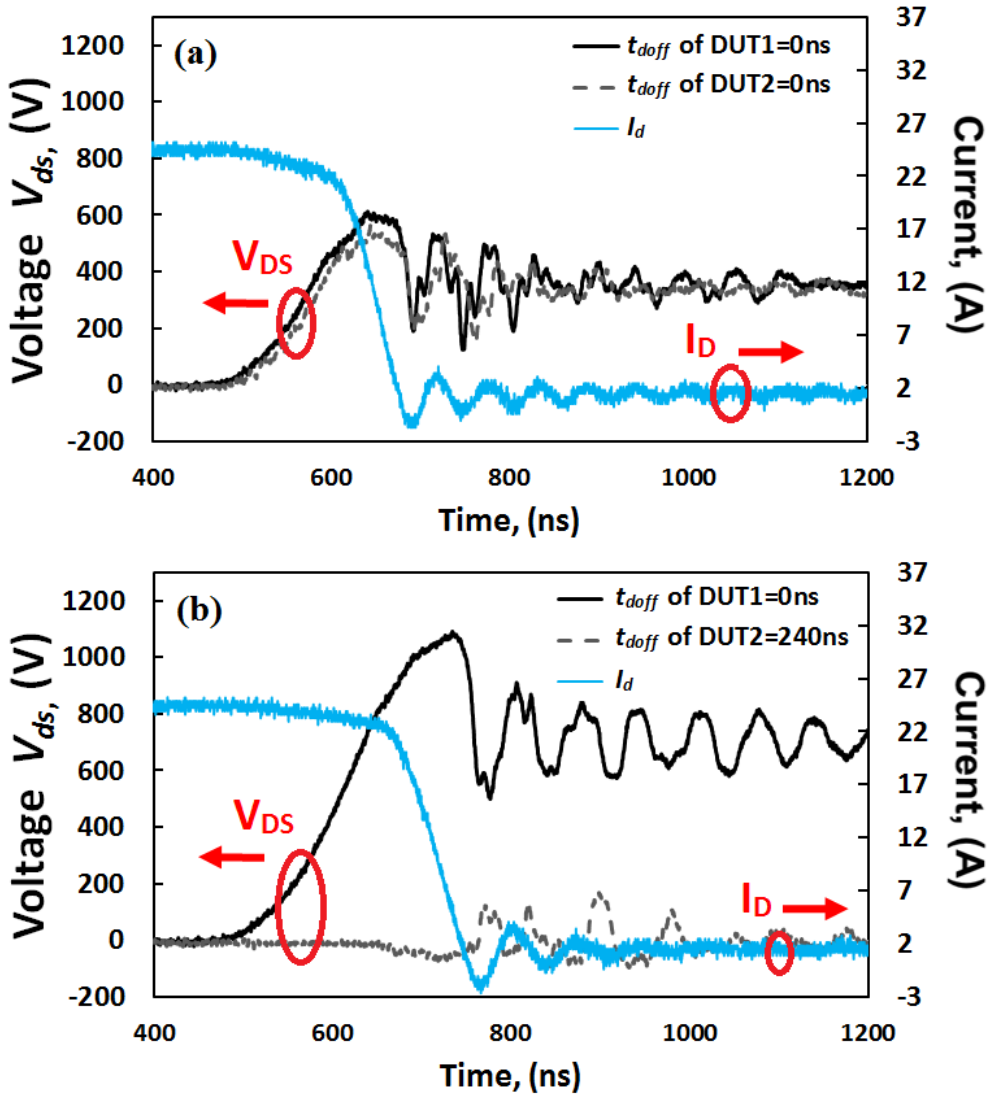


Fig. 5.9 Current and Voltage waveforms of series connected SiC trench MOSFETs during turn-OFF with (a) perfectly synchronized gates and (b) 240 ns gate delay leading to avalanche breakdown.

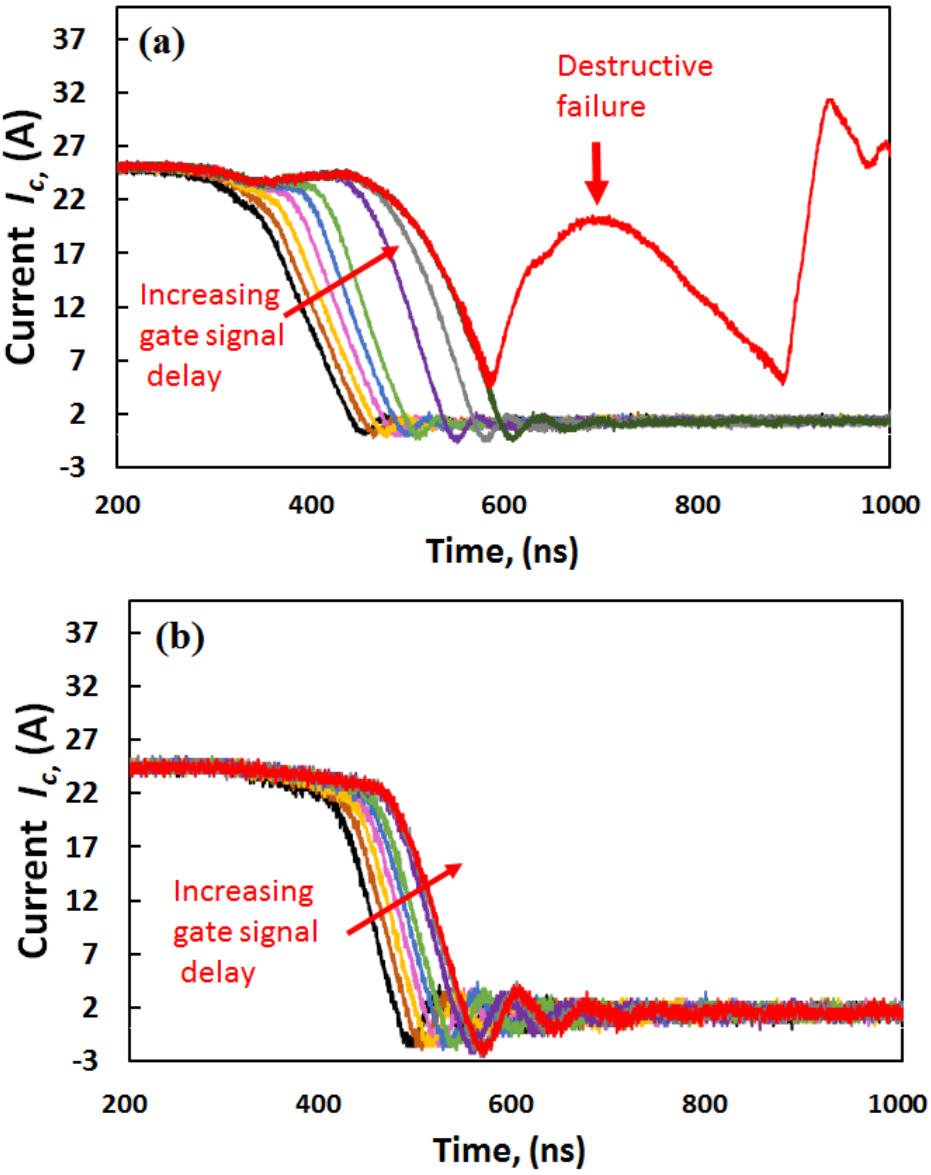


Fig. 5.10 The turn-OFF current waveforms through the series connected devices for different gate signalling delay for the (a) silicon IGBT and (b) SiC MOSFET.

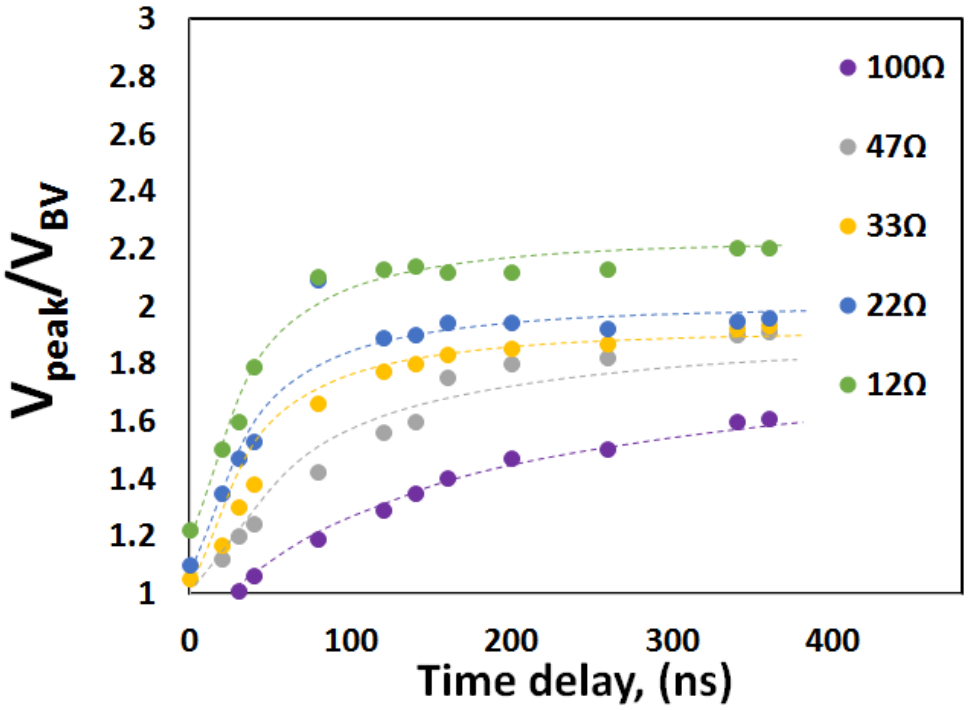


Fig. 5.11 Ratio peak measured voltage to rated breakdown voltage of SiC MOSFET as a function of the gate signalling delay at 700V.

The measurements of the turn-OFF transient for series connected MOSFETs that were done for several switching rates is shown in Fig. 5.11 for a DC link voltage of 700V. Fig. 5.11 shows the ratio of the peak measured voltage to the breakdown voltage of the device as a function of switching rate and the maximum gate mismatch delay before failure under latch-up.

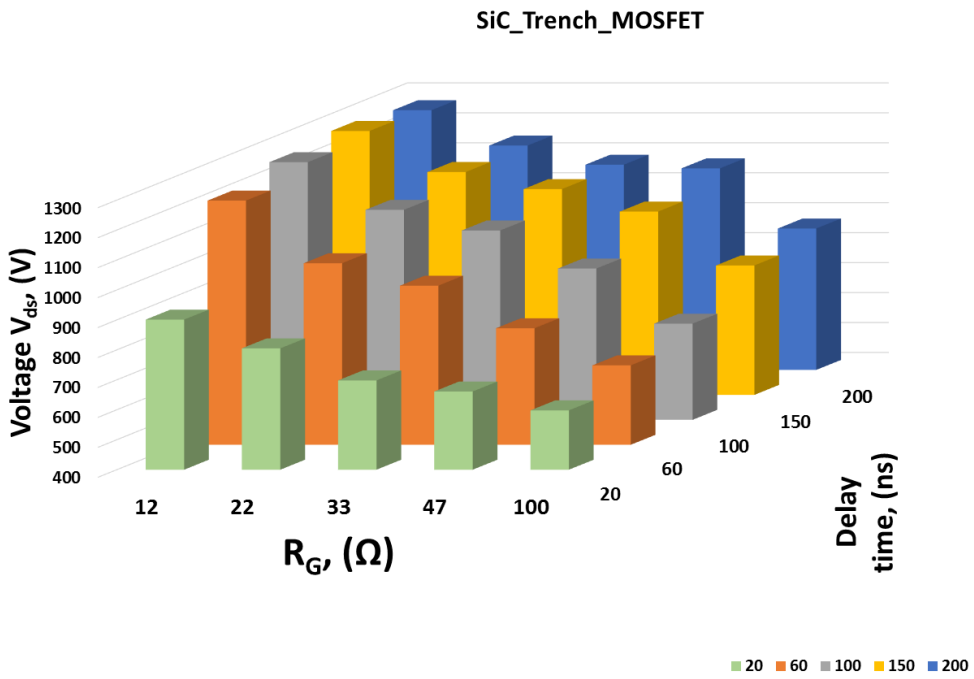


Fig. 5.12 Voltage rise look up table for series connected SiC MOSFETs switched with different gate resistances and time delays.

Fig. 5.12 shows a 3D graph of the drain-source peak voltage overshoot during the switching transient of two series connected devices against different gate resistances and different gate delays. As can be seen, by increasing the gate trigger delay, using the same gate resistor, the voltage overshoot increases. Also, it can be seen that with reduction of the gate resistor, at a constant gate delay, the voltage overshoot increases. Additionally, the percentage rise of the voltage overshoot when the gate resistor is reduced from 22Ω to 12Ω is less than the percentage rise of the overshoot when the gate delay is increased from 20ns to 60ns for SiC MOSFET indicating that this device is more sensetive to gate trigger delay rather than the gate resistance.

Fig. 5.13 shows the similar 3D graph of voltage overshoot rise against gate resistance and gate trigger delay. In contrast to SiC graph, the voltage overshoot is more sensetive to the gate resistance rather than the gate delay. This is due to the fact that Si IGBTs are intrisincly slower than SiC MOSFETs and the dV/dt (switching rate) of them are more dependent on the gate resistance.

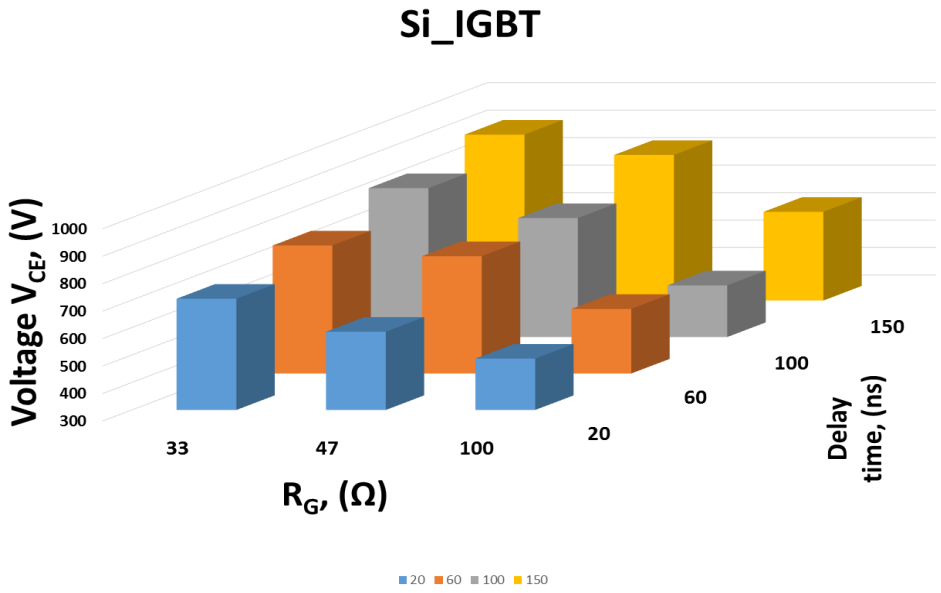


Fig. 5.13 Voltage rise look up table for series connected Si IGBTs switched with different gate resistances and time delays.

5.5 Finite Element Modelling and Simulation Results

Finite element simulations using SILVACO TCAD have been performed to validate the failure hypothesis of IGBT during transient switching under clamped inductive load. The circuit shown in Fig. 5.4 (a) has been simulated in ATLAS from SILVACO using the mixed mode circuit application to solve the switching transients with the finite element model. In addition to the components shown in Fig. 5.4 (a), the parasitic inductances of the circuit (stray inductance, parasitic inductance of the emitter as well as the gate) were also considered to provide a more representative switching waveform in the simulation. This improves the switching behaviour and creates a more detailed model of the experiment; however, it dramatically increases the simulation time. Finite element simulations have been performed on Si IGBTs and SiC MOSFETs under clamped inductive load to gain a deeper insight into the physics of device failure with two series connected devices.

5.5.1 Series Connected Si IGBTs

The silicon IGBT is simulated with a drift layer doping of 1×10^{14} cm^{-3}, a p-body doping of 7×10^{16} cm^{-3}, buffer layer doping of 1×10^{18} cm^{-3} and a voltage blocking drift layer thickness of 83 µm. Fig. 5.14 shows the cross-section view of Si IGBT which was

modelled in SILVACO and the vertical cut-line through the channel under the gate to the p-body down to the collector of the device. Fig. 5.15 shows the simulated voltage transients for the series connected IGBTs switched at different gate delays (0ns, 300ns).

Fig. 5.15 shows the simulated voltage and current transient of the series connected silicon IGBTs extracted from the mixed-mode circuit in SILVACO. It can be seen from Fig. 5.15 that that the simulated collector voltage divergence rates between the series devices replicate the experimental measurements shown in Fig. 5.15 (b). Seven points in the transient waveform have been identified as can be seen below. The internal electric field along the cross-section of the device (shown along the cut-line in Fig. 5.14) is extracted at these time intervals to show the internal fields during turn-OFF. At point t5 in Fig. 5.15, the maximum blocking voltage of the IGBT is reached. In FEM of a Trench Si-IGBT, modelling the failure was not possible, since the trench setup is a very robust structure against thyristor latch-up. In addition, in experimental IGBTs (where thousands of internal cells conduct current in parallel) where several IGBT cells are paralleled in the main device, failure would occur before this point due to current non-uniformity and localized hot spot in the device which results in an uncontrolled electron-hole pair generation [15].

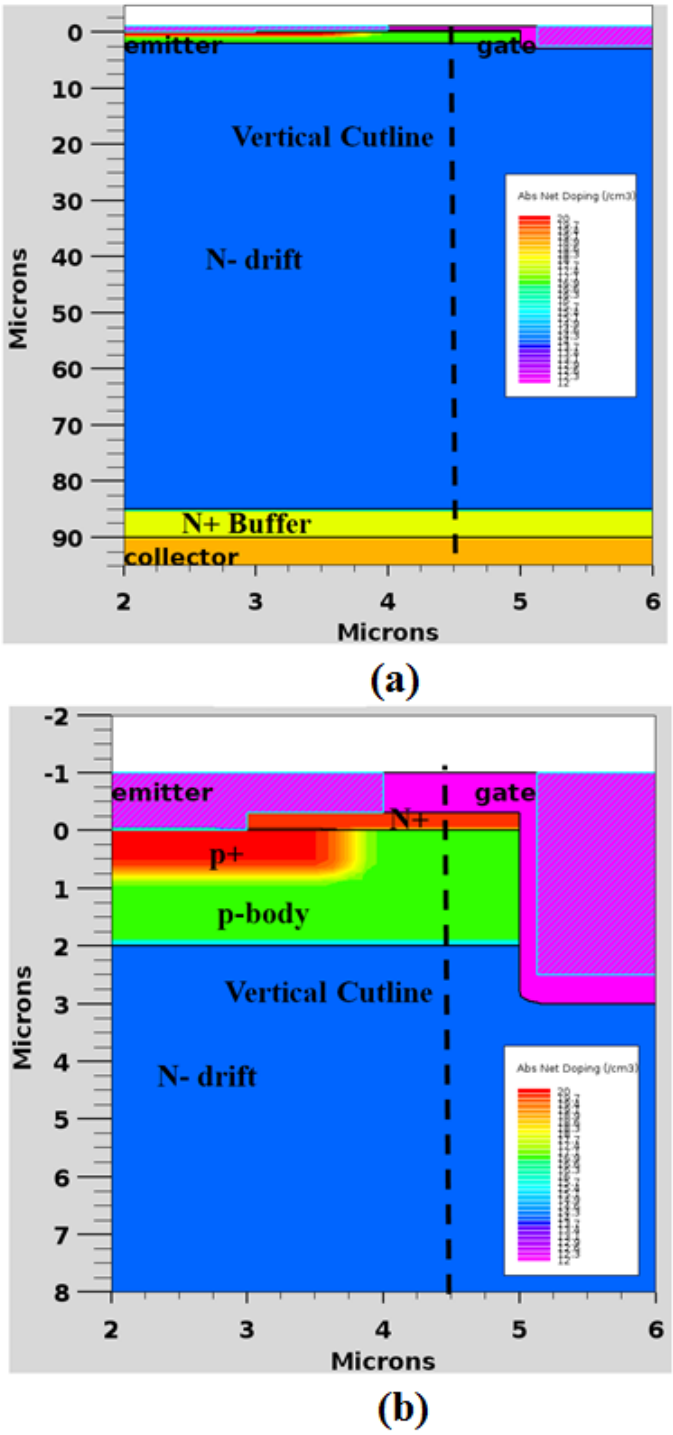


Fig. 5.14 (a) cross section view of the overall structure of the device (b) magnified cross section view of top of the emitter and gate configuration.

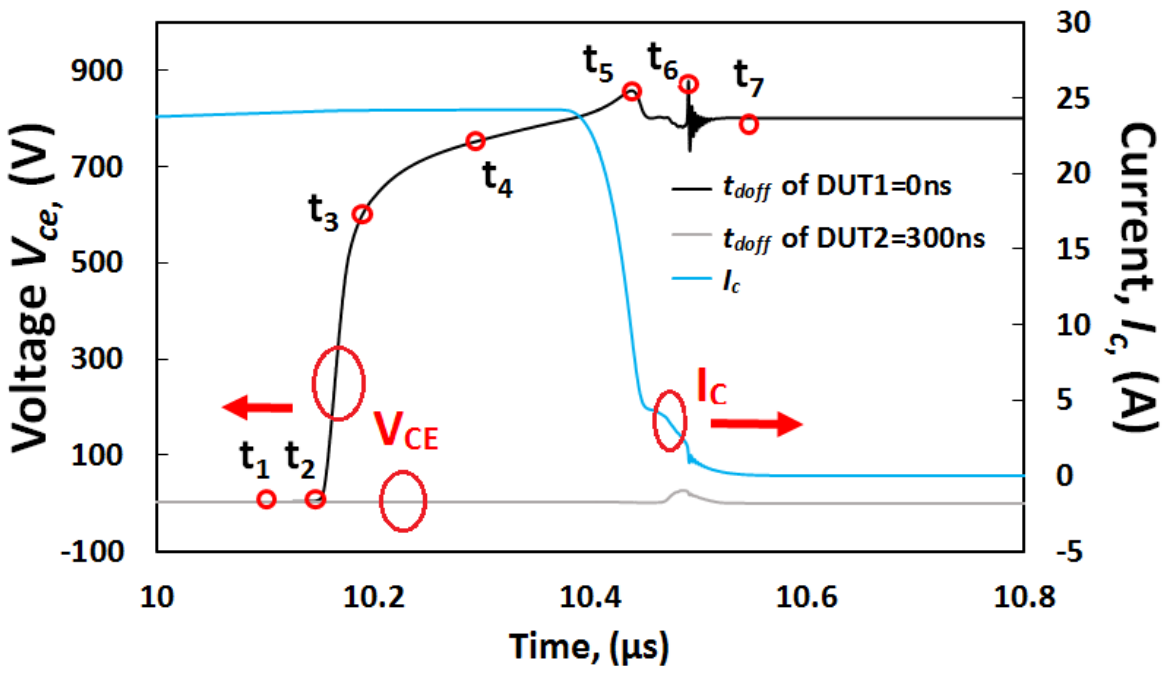


Fig. 5.15 The simulated current and voltage waveforms of series connected Si IGBTs during turn-OFF with 300 ns gate delay leading to avalanche breakdown.

Fig. 5.16 (a) and Fig. 5.16 (b) show the simulated internal electric field across the fast and slow IGBT at different stages of the turn-OFF transient, as it blocks voltage across the reverse biased PN junction. As can be seen, the electric field across the drift region of the fast IGBT builds up at a significantly higher level than the slower IGBT. This explains the higher voltage across this device during the switching transient. At t6, the channel at the bottom device is off and the current drops rapidly. This coupled with the stray inductance of the device, creates a sudden rise in the voltage. Between time t6 and t7, the electric field punches through to the buffer layer of the IGBT for the faster device. The displacement current through the P-well of the fast IGBT between these

two points creates a voltage at the gate of the parasitic NPN BJT within the IGBT structure. If this voltage exceeds the built-in voltage of the junction, the parasitic thyristor can latch-up.

The fast switching IGBT, as shown in Fig. 5.16 (a) has an internal electric field that spreads across the device and depletes holes from the drift region. In the slow switching IGBT shown in Fig. 5.16 (b), the internal electric field is at a minimum, hence, there is no depletion of holes from the drift region.

The hole concentration profile at different time steps shows the process of formation of depletion region during the switching transient in Fig. 5.17 (a) and (b). It can be seen that the faster device is depleted quicker, the depletion region forms completely in this device whereas in the slower device there are some charge still remaining in this region. Hence, the faster device has higher blocking voltage. The parameter that contributes the most in this process is the minority carrier lifetime in the drift region of the device. With higher carrier lifetime, the carrier concentration in the drift region during the switch-off process becomes higher. This leads to excessive amount of holes to be stored which needs to be extracted. As explained earlier, as the electric field builds up across the length of the device, and as it reaches the critical electric field of the device, with presence of holes across the drift layer of the device, an uncontrolled generation of electron and hole may happen which leads to the destruction of the device.

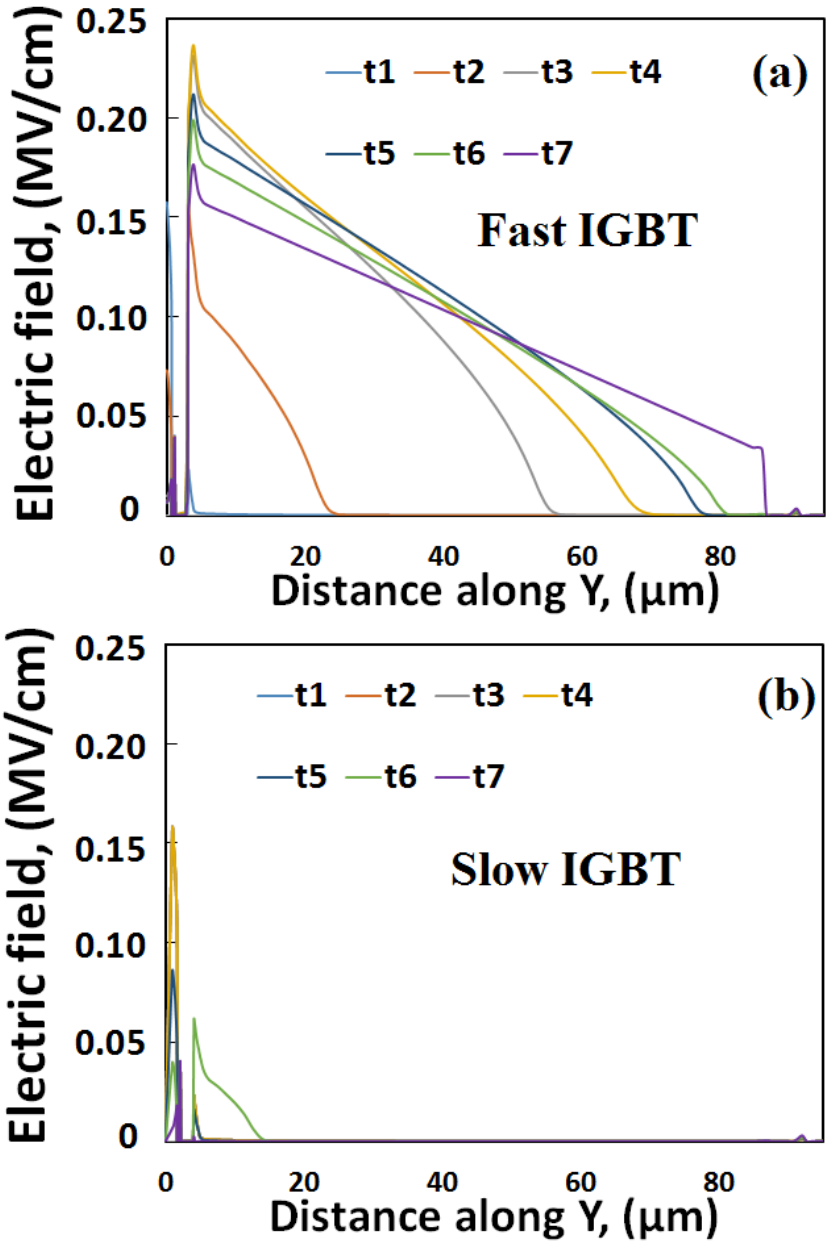


Fig. 5.16 Internal Electric field simulation (a) fast IGBT (b) slow IGBT

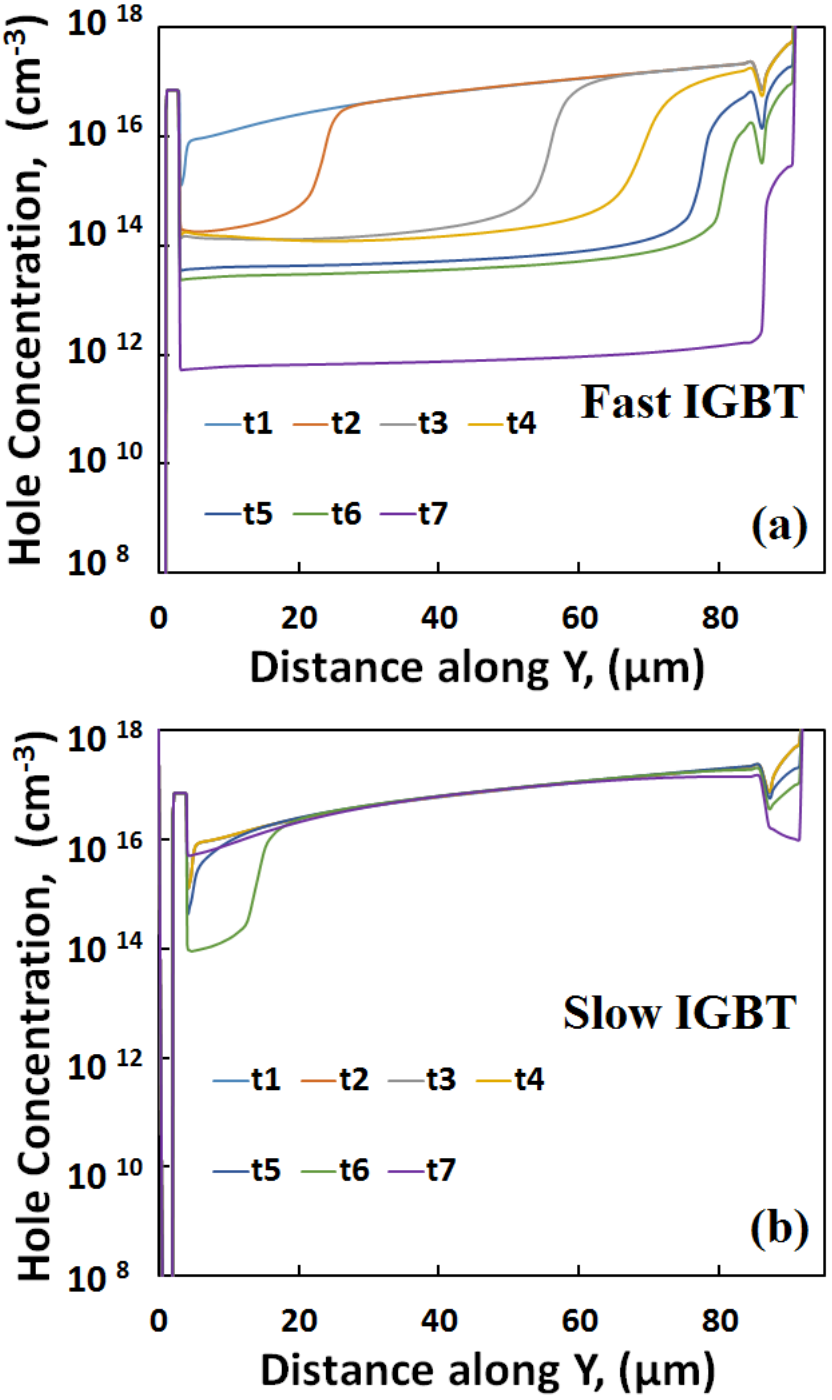


Fig. 5.17 Hole concentration simulation (a) fast IGBT (b) slow IGBT

Trench IGBT structure is very immune against latching with appropriate distance between p-body and trench [31]. However, by increasing temperature, the latch-up can occur during the transient switching. Single cell simulations were performed at temperature of 125°C. The results are shown in Fig. 5.18, where the transient CIS characteristics can be seen for series connected devices at 125°C during which both devices undergo the parasitic bipolar latch-up. Different points in the latch-up transient have been labelled (W, X, Y and Z). Device cross-sections of the DUT have been extracted from the simulator at the time instants corresponding to points W, X, Y and Z.

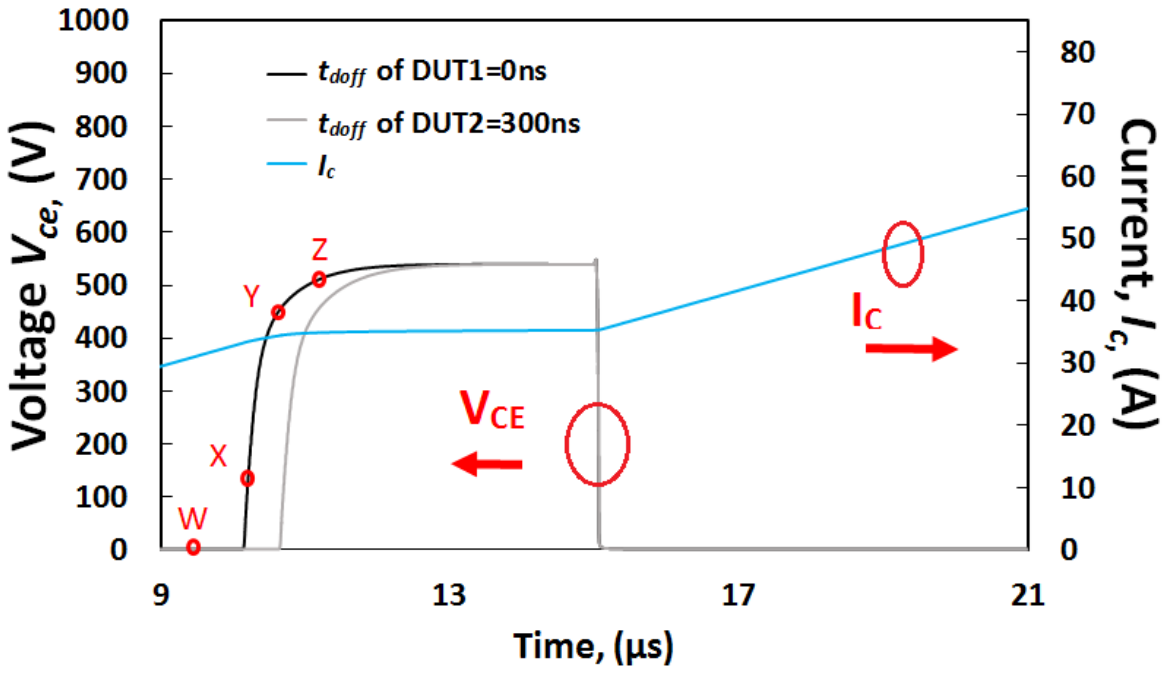


Fig. 5.18 Simulated latch-up current and voltage characteristics at 125°C.

Fig. 5.19 shows the potential of both devices at the corresponding time instants. As it was discussed before the hole current component travels laterally through the p-type body layer. This current flow will result a voltage drop in the ohmic resistance of the p-body layer. This can forward bias the N+P junction with the largest voltage across the junction. If the voltage is large enough, then parasitic npn BJT can switch on. If this happens, then both the parasitic pnp and npn BJTs are forward biased, and parasitic thyristor will latch-on and the latch-up of IGBT will occur [32]. At higher temperatures even the smaller current can create a large enough voltage to trigger the latch-up. In addition, the built-in voltage reduces with increased temperature, making the device more prone to latch-up. This is due to the increase of the intrinsic carrier concentration at elevated temperatures. Fig. 5.19 (a) and (b) show the 2-dimensional potential plots of the faster and slower devices respectively at different points corresponding to Fig. 5.19. At point W, the devices are switched ON. At point X, only faster device latches-up, since the potential in p-body region is higher than in N+ region as shown in Fig. 5.19 (a). At points Y and Z, both devices undergo the latch-up.

Fig. 5.20 (a) and (b) presents the simulated 2-dimensional electron current density of faster and slower series connected devices at 125°C. As can be seen at point W both devices have electron current flowing through the channel while at point X the electron current can be observed only in DUT 2. Then the channel cuts off and as shown in Fig. 5.20 (a) and (b) no longer electron current flows through both devices at points Y and Z.

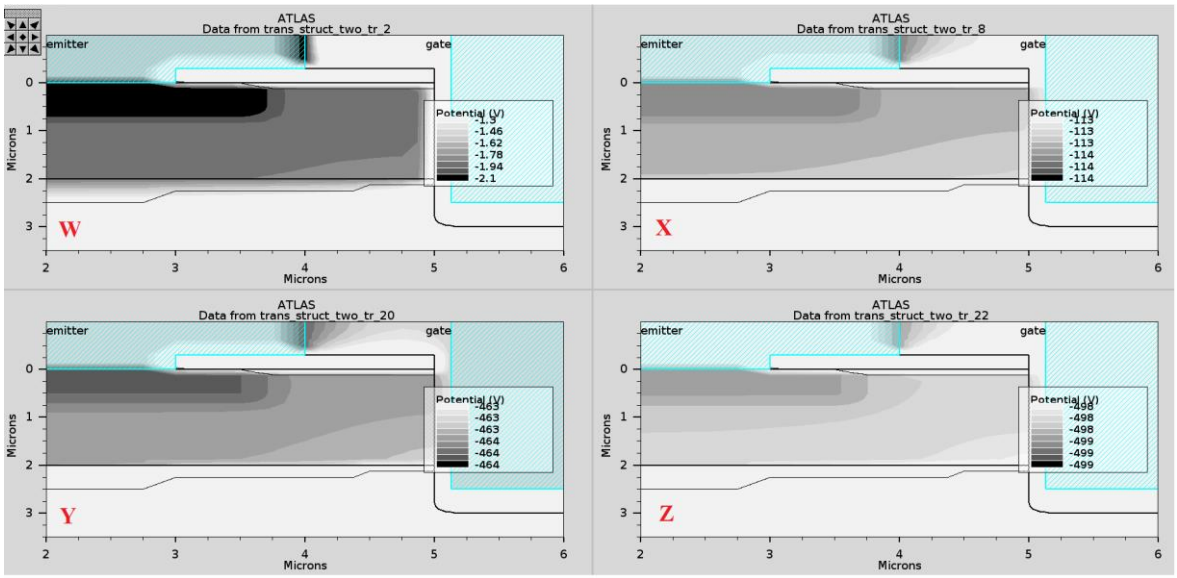
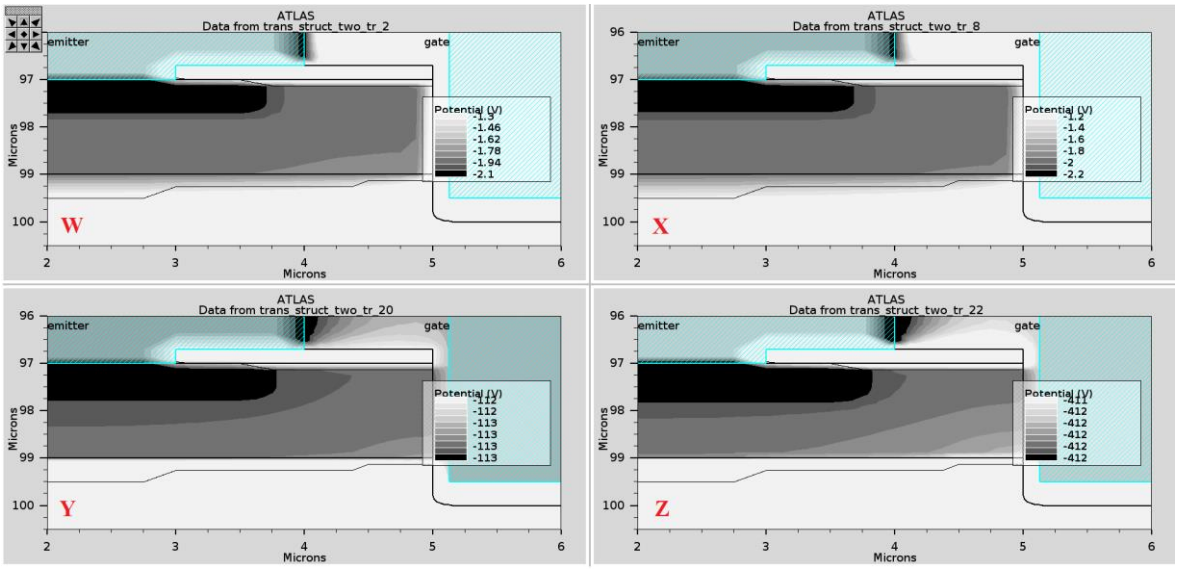


Fig. 5.19 (a) Simulated potential of DUT1 without delay



(b) Simulated potential of DUT2 with 300ns delay

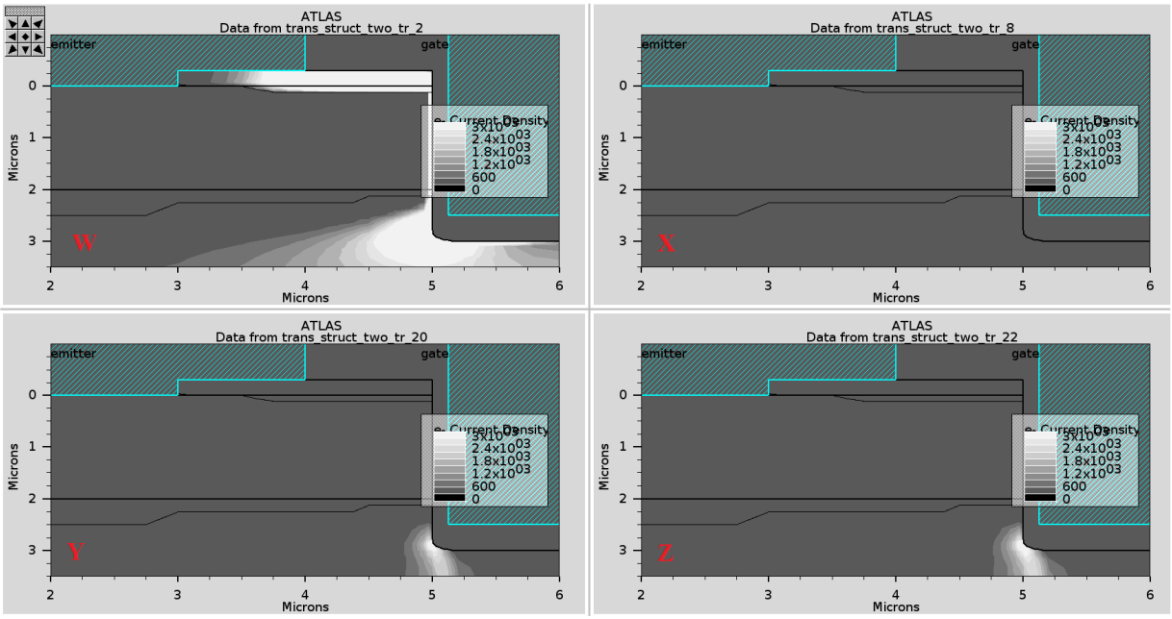
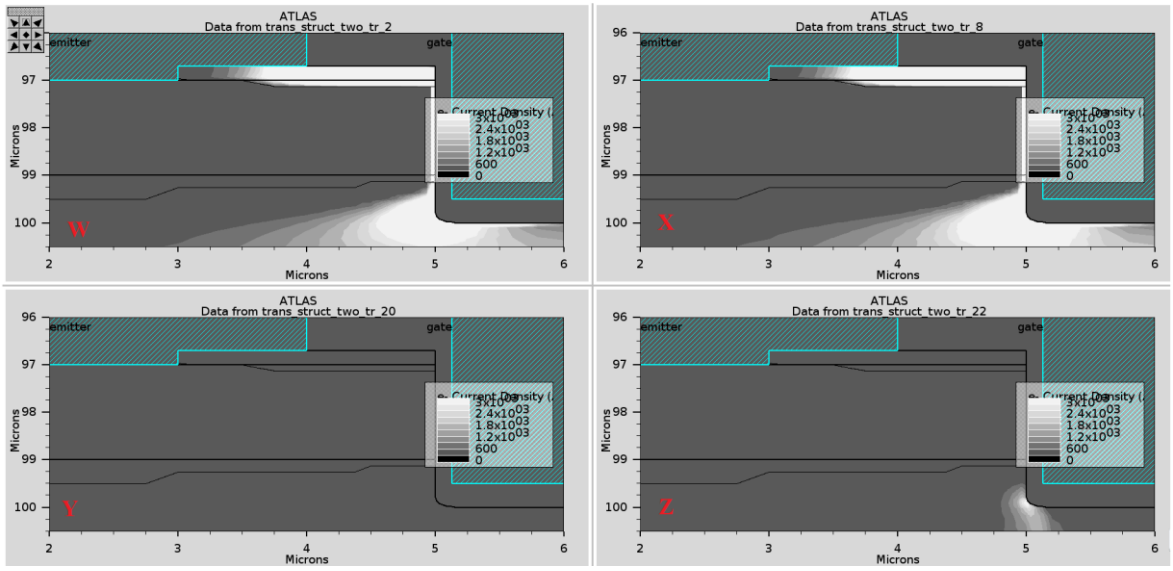


Fig. 5.20 (a) Simulated electron current density of DUT1



(b) Simulated electron current density of DUT2

Figure 5.21 (a) and (b) shows the simulated 2-dimensional hole current density of faster and slower series connected devices at 125°C. As can be observed at point X there is a significant hole current flow through the p-type body layer in DUT1, which indicates

the start of latch-up, whereas DUT 2 doesn't have the same level of hole current through the p-body layer. At points Y and Z there are presence of hole current in both devices.

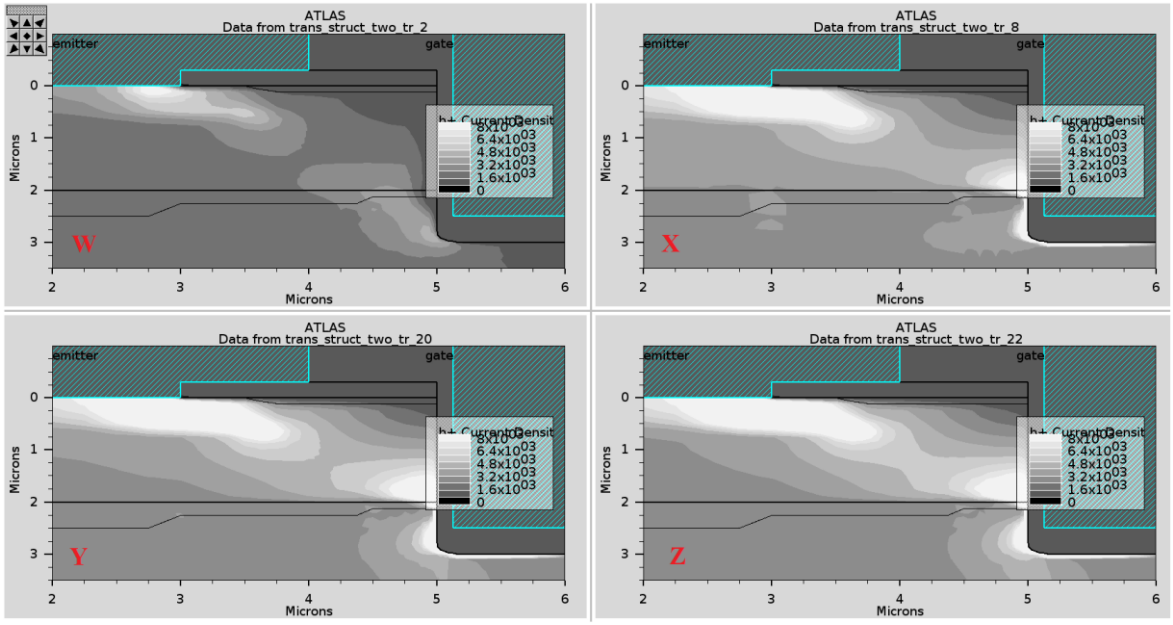
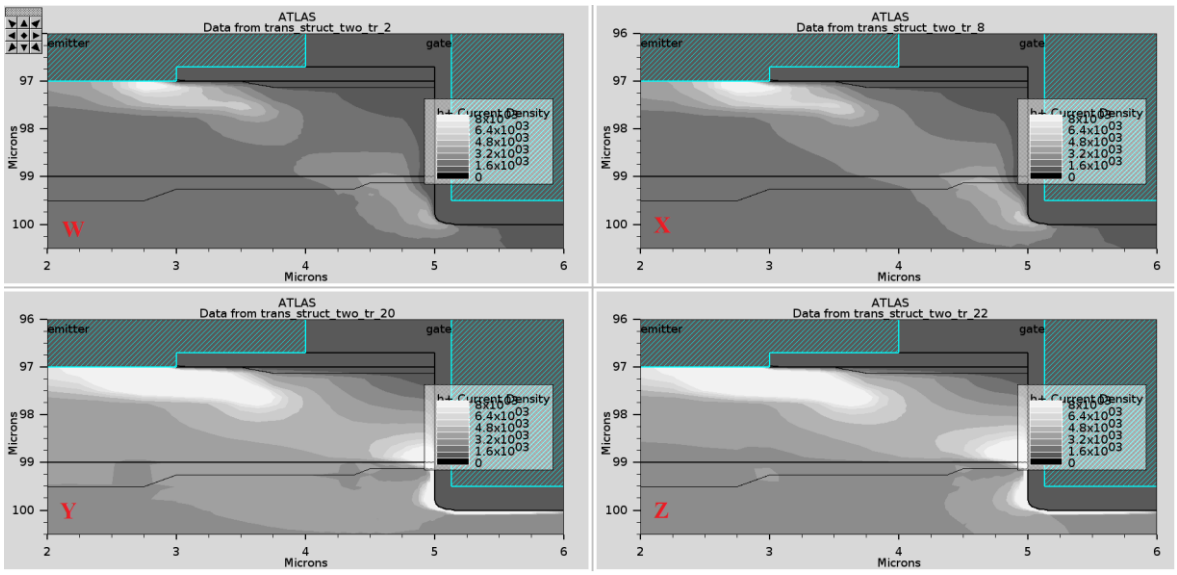


Fig. 5.21 (a) Simulated hole current density of DUT1



(b) Simulated hole current density of DUT2

5.5.2 Series Connected SiC MOSFETs

The SiC device in the simulation was optimized to a breakdown voltage of 1200 V using a ~9 µm depletion layer with a doping of 2×10^{16} cm^{-3}. A gate oxide thickness of 80 nm, a source doping of 1×10^{18} cm^{-3} and p-body doping of 1×10^{17} cm^{-3} was used in the simulation. The leakage current of a 650V rated SiC MOSFET was measured and the breakdown voltage of the device was measured to be 1.2 kV. Similarly, the IGBT was designed to show a breakdown voltage of 900V as the leakage current measurement indicated that the real breakdown voltage of the device was 900V. Fig. 5.22 shows the cross-section view of a trench SiC MOSFET structure. The vertical dashed line shown in this figure is used to show the electric field across the two series connected devices during the unbalanced switching of the devices. The parasitic inductance of the model was optimized to make the voltage ringing more representing to the experiments.

The simulated voltage and current turn-OFF transients as shown in Fig. 5.23 where significant ringing in the output characteristics can be observed. This is due to resonance between the parasitic capacitance in the SiC MOSFET and the parasitic inductance added to emulate the package inductance. Ringing in SiC MOSFETs is a well characterized switching hazard [28].

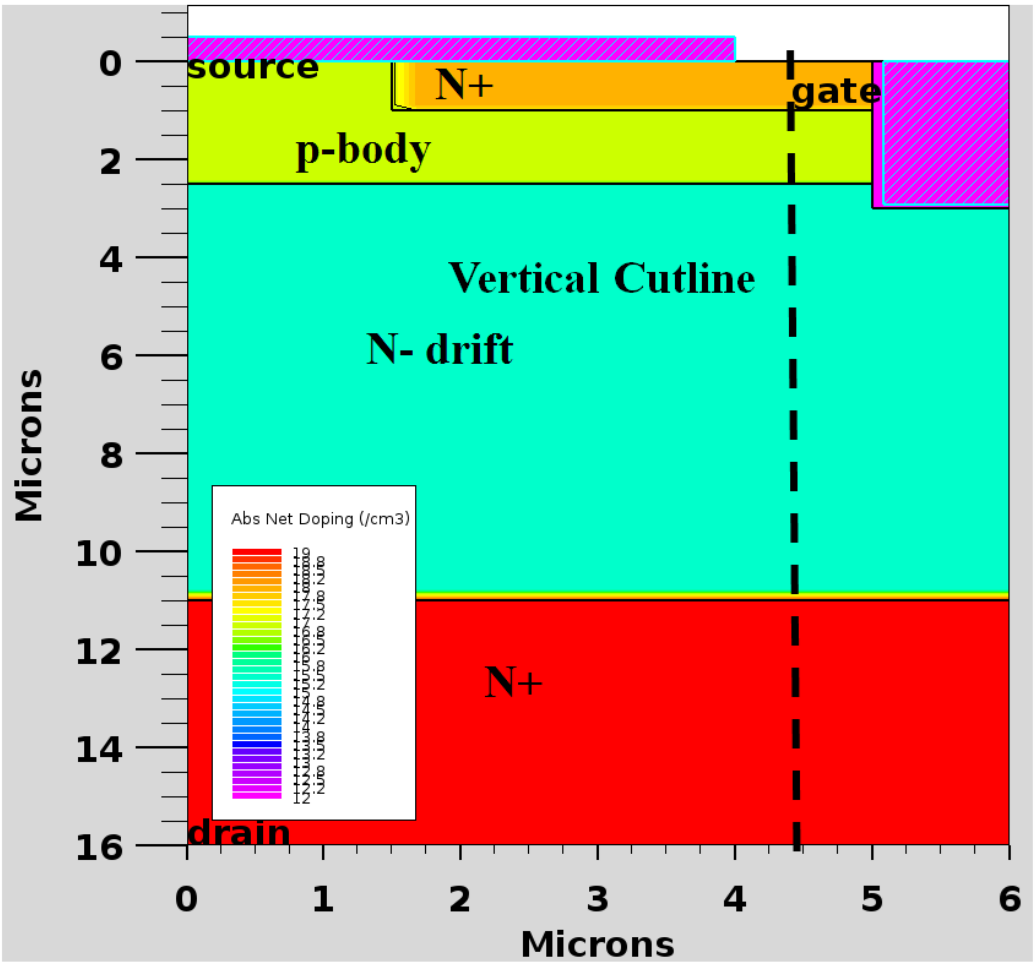


Fig. 5.22 SiC Trench MOSFET model rated at 1200V.

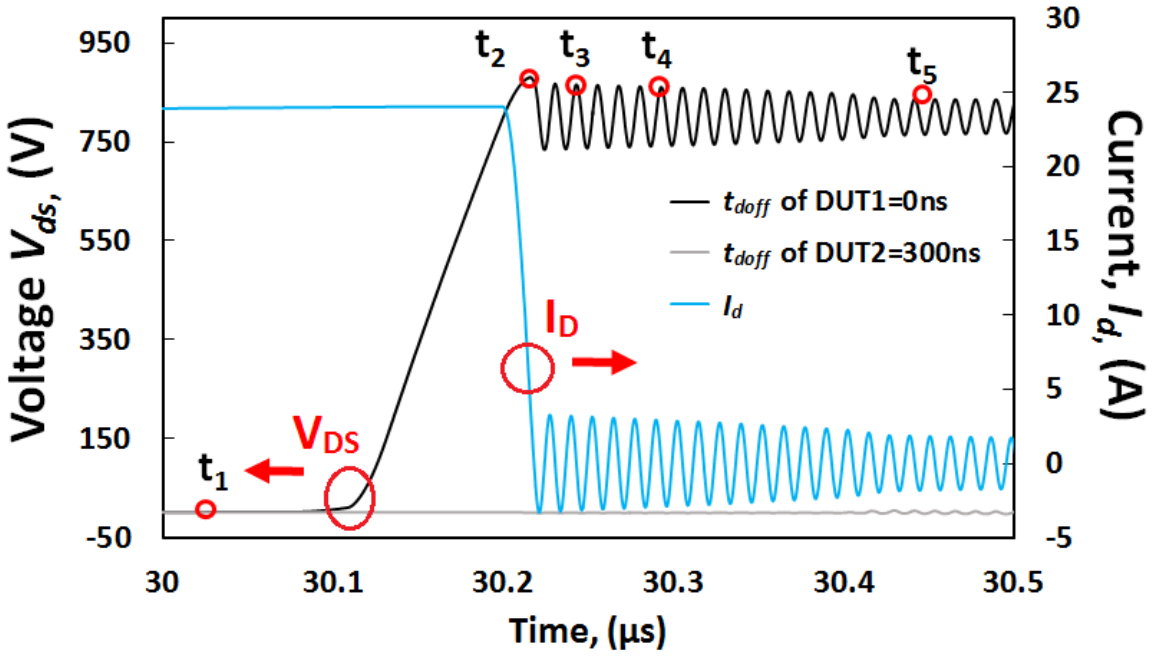


Fig. 5.23 The simulated current and voltage waveforms of series connected SiC MOSFETs during turn-OFF with 300 ns gate delay.

Fig. 5.24 shows the simulated internal electric fields of the series connected SiC trench MOSFETs. The internal electric fields were extracted along the vertical cross-section of the SiC MOSFET at the time intervals t1 to t5 shown in Fig. 5.24. Like the Si IGBTs, the fast switching device has a higher internal electric field compared to the slower switching device. It can also be observed that the electric fields in the SiC MOSFETs are much higher (approximately 10 times higher) that those in the Si IGBTs. This is due to the significantly thinner drift region in the SiC MOSFET that is enabled by the higher critical fields. This is an intrinsic property of SiC as a material. SiC MOSFETs have parasitic BJTs and not thyristors, hence, latch-up involves the triggering of the

internal NPN BJT. If during turn-OFF, the voltage limits of the device are exceeded, avalanche mode conduction will occur which may trigger NPN BJT latch-up.

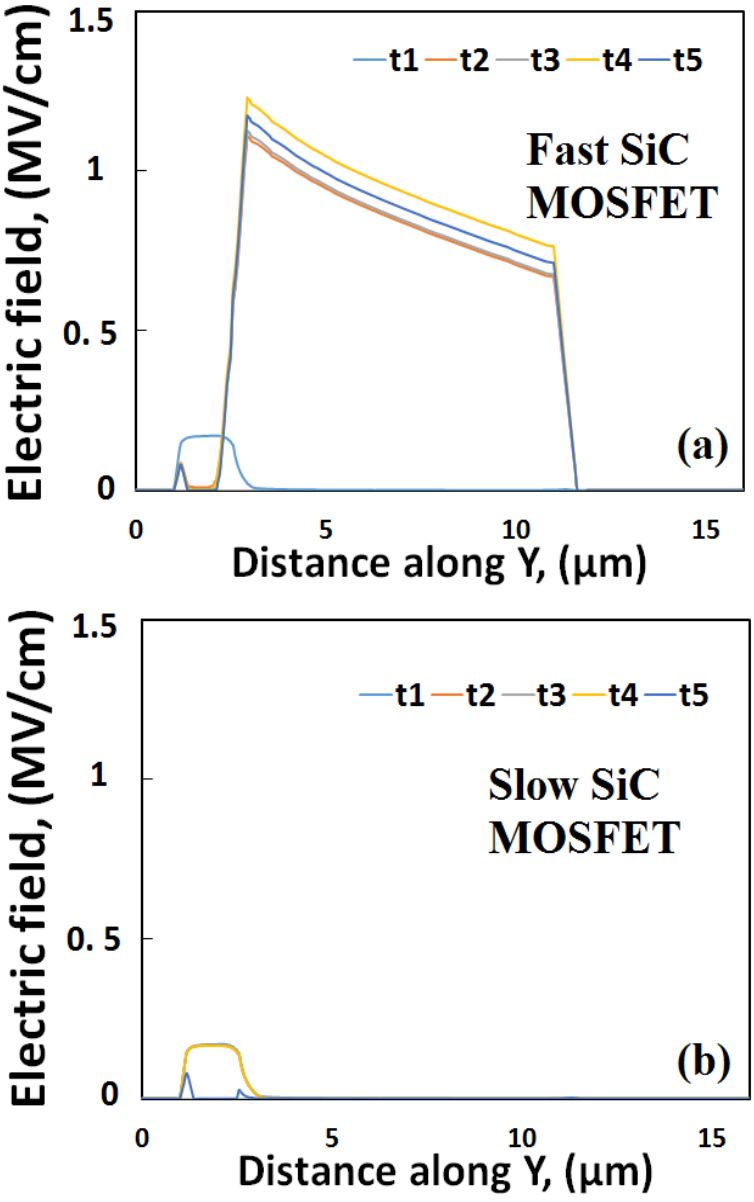


Fig. 5.24 Internal Electric field simulation (a) fast SiC MOSFET (b) slow SiC MOSFET

5.6 Conclusion

Series connected devices are used for blocking higher voltages. Snubbers are typically used for static and dynamic voltage balancing however active gate drive systems don't use snubbers, hence, it is important to develop a technique for determining the SOA for series connected devices. Gate timing mismatch (loss of gate synchronization) can cause destructive failure from avalanche conduction. Experimental measurements and simulations have been used to investigate the SOA of series connected silicon field-stop IGBTs and SiC trench MOSFETs. The SOA is reduced by increased switching rates and DC link voltages. For a given switching rate, the maximum gate mismatch between the series devices to trigger avalanche induced failure reduces with increasing DC link voltage. Likewise, for a given DC link voltage, the maximum gate mismatch delay for triggering avalanche mode failure reduces with increasing switching rate. Hence, as far as maximizing the SOA is concerned, there is a trade-off between the DC link voltage and the switching rate.

5.7 References

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Chapter

6 Loss Distribution in 3-Level NPC Converters with Silicon IGBT and SiC Power Devices

6.1 Introduction to 3-Level NPC Converters

While chapters 3, 4 and 5 considered the physics and operation of series connected IGBTs at the device level, this chapter looks at the loss distribution between the devices at converter level. Specifically, this chapter looks at the 3-level Neutral-Point-Clamped (NPC) converter which is an increasingly popular topology for medium voltage industrial AC drives, wind energy conversion systems and grid connected converters. In applications with higher DC link voltages where series connection of power devices is required for voltage sharing in the classical 2-level converter, the 3L-NPC is a good compromise between the simplicity of the 2L converter and the complexity of higher-level MMC converters [1]. The earliest HVDC-VSC systems comprised of a 2-level PWM VSC with series connected IGBTs for blocking the DC link voltage. The technology was commercialized by ABB before the more sophisticated modular multi-level converter (MMC). The move towards MMC

was based on the difficulties regarding active and dynamic voltage balancing in 2 level converters [2-4]. MMC levels basically comprise of series connected H-bridges each with a submodule capacitor that determines the voltage level of each submodule. This means that the power devices can be specified to block only the submodule voltage and since each submodule has a bypass mechanical switch and thyristor, there converter is inherently fault tolerant. A defective submodule can be isolated by simply using the bypass thyristor/switch to short the submodule. Multi-level converters can be diode clamped converters [5-7], flying-capacitor converters or modular multi-level converters [8]. The advantage of multi-level converters is due to the fact that series connection of power devices can be minimized or completely avoided. This is because the introduction of additional levels means that the voltage blocked per level is reduced, hence, single devices can be used in the case that commercial devices are readily available. If the voltage blocked per level is still higher that the highest voltage blocking capability of commercial devices, then the number of series devices needed per level is reduced. This has significant implications in terms of converter design since series connection of power devices requires bulky and lossy snubbers for static and dynamic voltage balancing [9]. Multi-level converters also come with the advantage of reduced output filtering requirements since the output waveform is more sinusoidal than the basic 2 level PWM waveform. The disadvantage of multi-level converters is the control since the switching of the devices has to be timed to produce the desired waveforms. Since the DC link voltage is divided into submodule voltages, the DC link capacitors are independently charged and discharged, thereby introducing the additional complexity of capacitor balancing [10].

Of all the multilevel converters, the most successful has been the 3-level NPC converter. In this converter, the DC link voltage is divided into 2 levels with the midpoint termed as a neutral point

[11]. Fig. 6.1 (a) shows a 2-level converter with series connected power switches (MOSFETs or IGBTs) while Fig. 6.1 (b) shows a 3L-NPC converter.

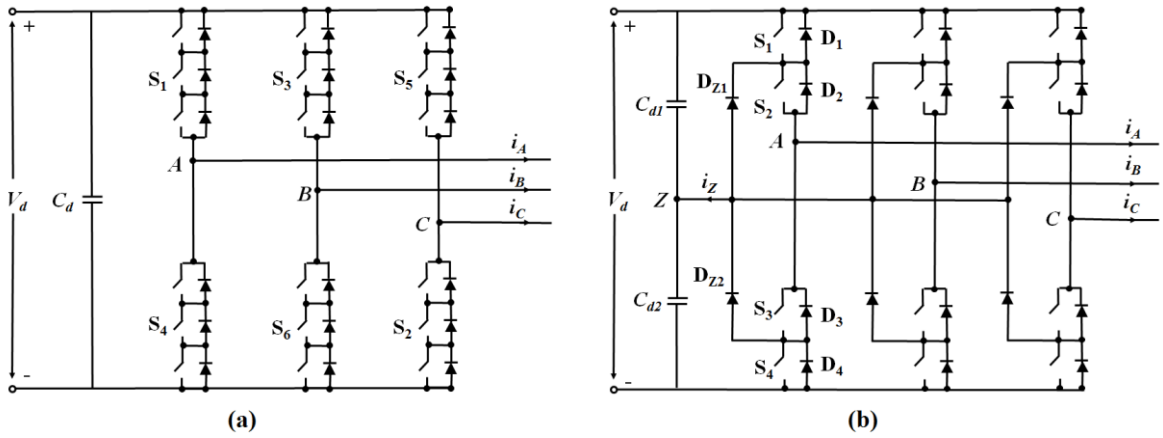


Fig. 6.1 (a) 2L 3-phase Voltage source converter and (c) 3L 3phase NPC Converter.

6.2 Operational and Control of the 3-L NPC Converter

While the phase voltage of the 2-level converter can be either at $+V_{DC}$ or $-V_{DC}$, the phase voltage in the 3L-NPC converter than have 3 levels, namely $+V_{DC}/2$, 0 and $-V_{DC}/2$. Hence, the line-to-line voltage of the 3L-NPC converter can have 5 levels namely, V_{DC}, $+V_{DC}/2$, 0, $-V_{DC}/2$ and $-V_{DC}$. Each phase of the 3L-NPC converter comprises of 4 bi-directional power switches and 2 clamping diodes. As a result, each phase can produce 3 distinct voltage levels as shown in Fig. 6.2 below. When the 2 upper devices are ON, the phase output is high ($+V_{DC}/2$), when the 2 middle devices are ON, the phase output is at 0

and when the 2 bottom devices are ON, the phase output is at ($-V_{DC}/2$). These can be respectively designated as P, O and N respectively. Fig. 6.3 shows how the current is conducted in each phase leg depending on the switching state of the phase leg and the direction of the current flow. To explain Fig. 6.3, it is first necessary to define positive current as current flowing from the DC side to the AC side and negative current as current flowing from the AC side to the DC side. The transistors are labelled as S1, S2, S3 and S4 with the outer transistors labelled as S1 and S4 and the inner transistors as S2 and S3. The clamping diodes that connect the converter phase output to the neutral point are labelled as D1 and D2.

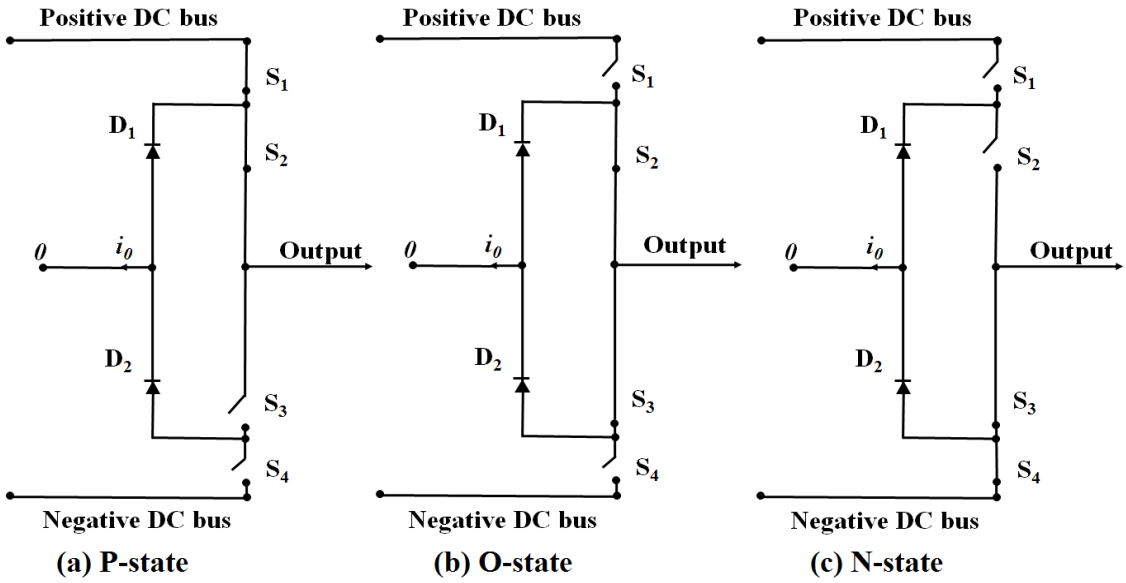


Fig. 6.2 Single phase of the 3L NPC Converter showing switching configurations.

Table 6.1 Switching state and corresponding voltage

Switching State	**Device Switching Status** (Phase *A*)				**Inverter Terminal Voltage** V_{AN}
	S_1	S_2	S_3	S_4	
P	On	On	Off	Off	E
O	Off	On	On	Off	0
N	Off	Off	On	On	$-E$

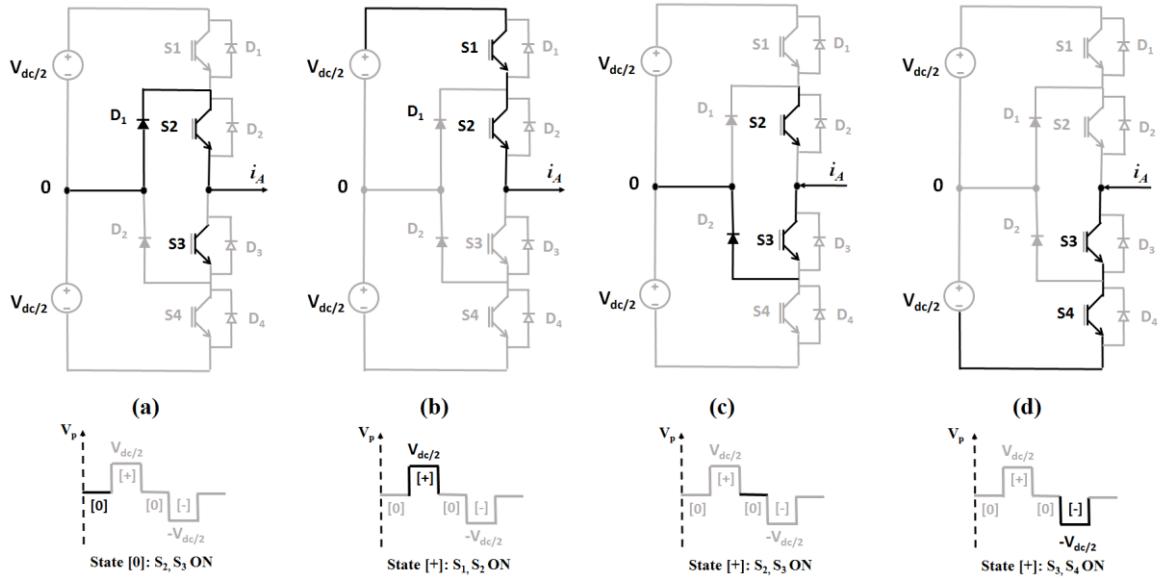


Fig. 6.3 (a) Phase voltage is 0 with positive current (b) Phase voltage is $+V_{DC}/2$ with positive current (c) Phase voltage is zero with negative current and (d) phase voltage is $-V_{DC}/2$ with negative current

Looking at Fig. 6.3 (a), when there is a positive current flowing and the phase output voltage is at zero, then the inner transistor (S3) and upper clamping diode (D1) conduct current. In Fig. 6.3 (b), it can be seen that when the phase output voltage is at $+V_{DC}/2$ and the current is positive, the 2 upper transistors (S1 and S2) conduct current. When the converter phase output voltage is at 0 and the current is negative, the inner transistor (S3) and clamping diode (D2) conductor current. When the current is negative and converter phase output voltage is at $-V_{DC}/2$, then transistors S2 and S3 conduct current. In general, the electrothermal stress within the converter will depend on which voltage switching vector is initiated and the direction of current flow at the time. In general, when the current is in phase with the voltage as is the case in a unity power factor load, the transistors bear the losses within the converter and when the current is out of phase with the voltage, the clamping diodes bear some of the losses [5,11].

Carrier-based 3-level PWM modulation is highly applied modulation methods in industry [12-13], which is based on the comparison of a sinusoidal reference voltage V_p with two carriers V_{cr1} and V_{cr2}. Figure 6.4 shows the carrier-based sinusoidal PWM. The logic of that modulation is quite straightforward:

If $V_p > V_{cr1}$ then S1 is ON, S2 is ON $V_{AN} = Vdc/2$

If $V_{cr2} < V_p < V_{cr1}$ then S3 is ON, S2 is ON $V_{AN} = 0$

If $V_p < V_{cr2}$ then S1 is ON, S2 is ON $V_{AN} = -Vdc/2$

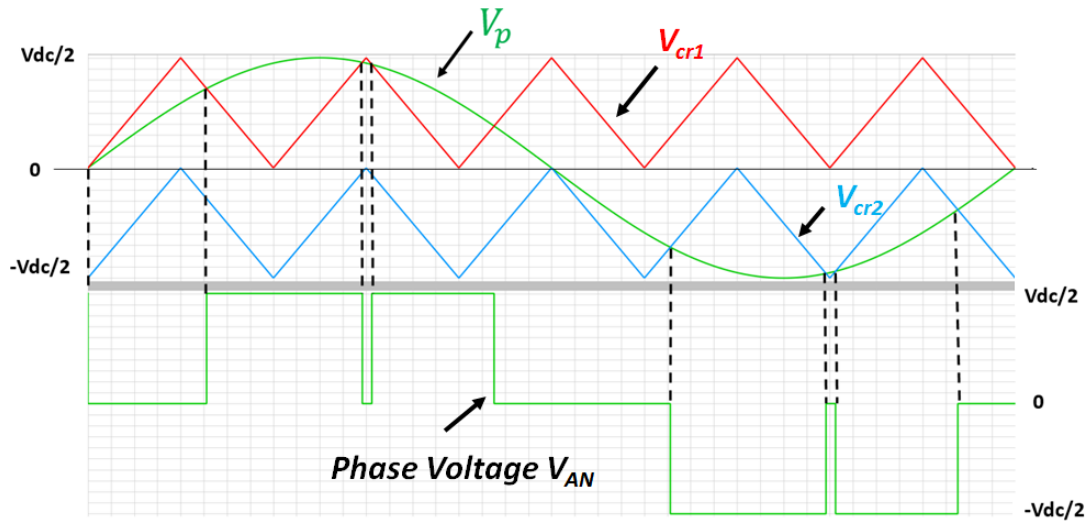
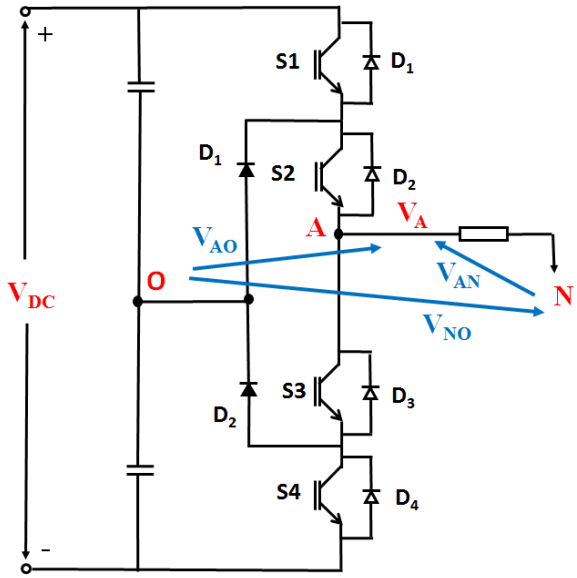


Fig. 6.4 Triangular-Sinusoidal PWM for 3-Level NPC inverter.

There is a continuous research on this modulation method in terms of optimal switching sequences [12], different modulation indexes [14], new topologies [15] and etc.

While the 2-level converter has 2^3=8 switching states (of which there are 6 active vectors and 2 zero vectors), the 3-level NPC converter has 3^3=27, switching states, of which 3 are zero vectors and 24 are active vectors. In defining a switching vector for the 2-level converter, a critical rule states that no 2 transistors in the same phase leg can be switched ON simultaneously, otherwise, the DC link capacitor is short circuited with potentially destructive consequences. Likewise, in the 3L-NPC converter, all the devices in a phase leg should not be turned ON. To define the converter phase voltages, line voltages and load phase voltages corresponding to a converter switching state, it is first necessary to consider a single phase of the converter, connected to a single phase of the load as shown in Fig. 6.5 below [16-19].



V_A = Converter output voltage

V_N = Load Neutral point

V_O = Converter Neutral point

V_{AN} = Load Phase Voltage

V_{AO} = Converter phase voltage

V_{NO} =Load Neutral to Converter Neutral Voltage

V_{DC} = DC link voltage

Fig. 6.5 Converter to load phase diagram

The load phase voltage is the voltage difference between the converter phase voltage and the "Load neutral to converter neutral voltage". This can be written for all phases.

$$V_{AN} = V_{AO} - V_{NO} \tag{6.1}$$

$$V_{BN} = V_{BO} - V_{NO} \tag{6.2}$$

$$V_{CN} = V_{CO} - V_{NO} \tag{6.2}$$

For a balanced 3 phase load, the sum of the phase voltages is equal to zero.

$$V_{AN} + V_{BN} + V_{CN} = 0 \tag{6.4}$$

Substituting for the load phase voltages

$$(V_{AO} - V_{NO}) + (V_{BO} - V_{NO}) + (V_{CO} - V_{NO}) = 0 \tag{6.5}$$

$$V_{NO} = \frac{1}{3}(V_{AO} + V_{BO} + V_{CO}) \tag{6.6}$$

$$V_{AN} = V_{AO} - \frac{1}{3}(V_{AO} + V_{BO} + V_{CO}) = \frac{2}{3}V_{AO} - \frac{1}{3}V_{BO} - \frac{1}{3}V_{CO} \quad (6.7)$$

The 3 line-to-line voltages at the converter output are

$$V_{AB} = V_{AO} - V_{BO} \quad (6.8)$$

$$V_{BC} = V_{BO} - V_{CO} \quad (6.9)$$

$$V_{AC} = V_{AO} - V_{CO} \quad (6.10)$$

For any one of the 27 converter switching states of the 3L-NPC, the converter phase voltage, load phase voltage and line voltage can be calculated. Each one of the switching states can be identified according to the converter phase voltages. For example, switching state PON means that the converter phase voltage A is at $+V_{DC}/2$, phase B is at 0 and phase C is at $-V_{DC}/2$. Likewise, switching state OPP corresponds to converter phase voltage A being 0, phase voltage B being $+V_{DC}/2$ and phase voltage C being $+V_{DC}/2$. If the switching state PON is taken hypothetically, then the load phase voltages be calculated as shown below

$$V_{AN} = \frac{2}{3}V_{AO} - \frac{1}{3}V_{BO} - \frac{1}{3}V_{CO} \quad (6.11)$$

Hence $V_{AN} = \frac{2}{3}\left(\frac{V_{DC}}{2}\right) - \frac{1}{3}(0) - \frac{1}{3}\left(-\frac{V_{DC}}{2}\right) = \frac{V_{DC}}{2}$; $V_{BN} = 0$ and $V_{CN} = -\frac{V_{DC}}{2}$

Table 6.2 below shows all 27 converter voltage switching states, with the corresponding line-to-line voltages and load phase voltages.

Table 6.2 27 switching states for the 3L-NPC Converter and the corresponding line voltages and load phase voltages.

No.	Switching state	Inverter phase voltage			Line-to-line voltages			Load neutral voltage	Load phase voltages		
		V_{Ao}	V_{Bo}	V_{Co}	V_{AB}	V_{BC}	V_{CA}		V_{An}	V_{Bn}	V_{Cn}
0	[NNN]	$-V_D/2$	$-V_D/2$	$-V_D/2$	0	0	0	$-V_D/2$	0	0	0
	[OOO]	0	0	0				0			
	[PPP]	$V_D/2$	$V_D/2$	$V_D/2$				$V_D/2$			
1	[POO]	$V_D/2$	0	0	$V_D/2$	0	$-V_D/2$	$V_D/6$	$V_D/3$	$-V_D/6$	$-V_D/6$
	[ONN]	0	$-V_D/2$	$-V_D/2$				$-V_D/3$			
2	[PPO]	$V_D/2$	$V_D/2$	0	0	$V_D/2$	$-V_D/2$	$V_D/3$	$V_D/6$	$V_D/6$	$-V_D/3$
	[OON]	0	0	$-V_D/2$				$-V_D/6$			
3	[OPO]	0	$V_D/2$	0	$-V_D/2$	$V_D/2$	0	$V_D/6$	$-V_D/6$	$V_D/3$	$-V_D/6$
	[NON]	$-V_D/2$	0	0				$-V_D/3$			
4	[OPP]	0	$V_D/2$	$V_D/2$	$-V_D/2$	0	$V_D/2$	$V_D/3$	$-V_D/3$	$V_D/6$	$V_D/6$
	[NOO]	$-V_D/2$	0	0				$-V_D/6$			
5	[OOP]	0	0	$V_D/2$	0	$-V_D/2$	$V_D/2$	$V_D/6$	$-V_D/6$	$-V_D/6$	$V_D/3$
	[NNO]	$-V_D/2$	$-V_D/2$	0				$-V_D/3$			
6	[POP]	$V_D/2$	0	$V_D/2$	$V_D/2$	$-V_D/2$	0	$V_D/3$	$V_D/6$	$-V_D/3$	$V_D/6$
	[ONO]	0	$-V_D/2$	0				$-V_D/6$			
7	[PON]	$V_D/2$	0	$-V_D/2$	$V_D/2$	$V_D/2$	$-V_D$	0	$V_D/2$	0	$-V_D/2$
8	[OPN]	0	$V_D/2$	$-V_D/2$	$-V_D/2$	V_D	$-V_D/2$	0	0	$V_D/2$	$-V_D/2$
9	[NPO]	$-V_D/2$	$V_D/2$	0	$-V_D$	$V_D/2$	$V_D/2$	0	$-V_D/2$	$V_D/2$	0
10	[NOP]	$-V_D/2$	0	$V_D/2$	$-V_D/2$	$-V_D/2$	V_D	0	$-V_D/2$	0	$V_D/2$
11	[ONP]	0	$-V_D/2$	$V_D/2$	$V_D/2$	$-V_D$	$V_D/2$	0	0	$-V_D/2$	$V_D/2$
12	[PNO]	$V_D/2$	$-V_D/2$	0	V_D	$-V_D/2$	$-V_D/2$	0	$V_D/2$	$-V_D/2$	0
13	[PNN]	$V_D/2$	$-V_D/2$	$-V_D/2$	V_D	0	$-V_D/2$	$-V_D/6$	$2V_D/3$	$-V_D/3$	$-V_D/3$
14	[PPN]	$V_D/2$	$V_D/2$	$-V_D/2$	0	V_D	$-V_D$	$V_D/6$	$V_D/3$	$V_D/3$	$-2V_D/3$
15	[NPN]	$-V_D/2$	$V_D/2$	$-V_D/2$	$-V_D$	V_D	0	$-V_D/6$	$-V_D/3$	$2V_D/3$	$-V_D/3$
16	[NPP]	$-V_D/2$	$V_D/2$	$V_D/2$	$-V_D$	0	V_D	$V_D/6$	$-2V_D/3$	$V_D/3$	$V_D/3$
17	[NNP]	$-V_D/2$	$-V_D/2$	$V_D/2$	0	$-V_D$	V_D	$-V_D/6$	$-V_D/3$	$-V_D/3$	$2V_D/3$
18	[PNP]	$V_D/2$	$-V_D/2$	$V_D/2$	V_D	$-V_D$	0	$V_D/6$	$V_D/3$	$-2V_D/3$	$V_D/3$

Rotating reference frame transformations are used to implement the control of the converter in motor drive and grid applications. In motor drive applications, the torque and speed of the motor is controlled while in grid applications, the active and reactive power is controlled. In reference frame transformation, a rotating 3 phase AC signal is converted first to a rotating 2 phase reference using the Clark transformation. The result of that transformation is referred to as the alpha-beta (αß). After the Clark

transformation, the rotating 2 phase signal is converted to a stationary 2 phase signal using the Park transformation. This enables the control to be performed as DC quantities in a frame referred to as the dq frame.

To understand the operation of the Clark and Park transformations [19-20], it is necessary to first consider the reference voltage vector, which is a resultant of the 3 voltage vectors

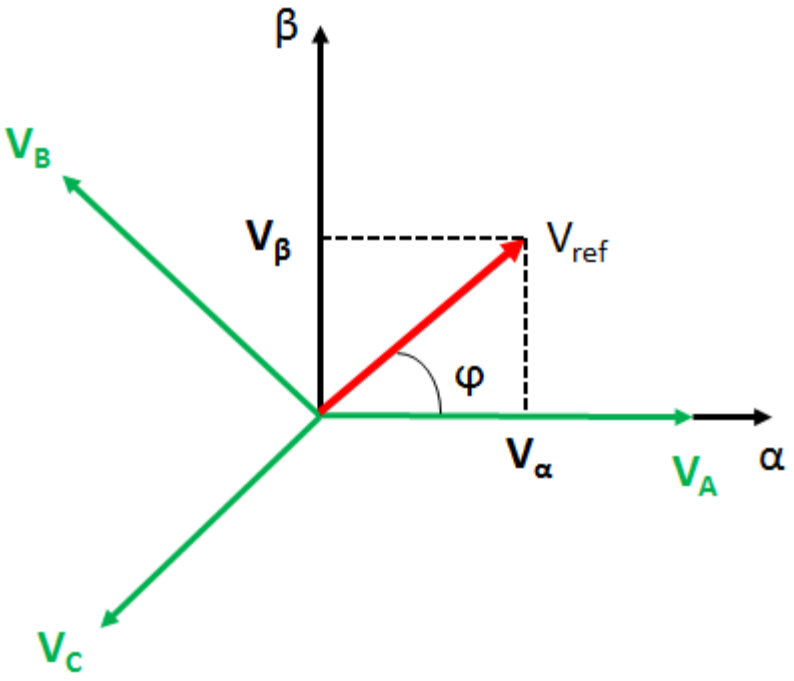


Fig. 6.6 Conversion of 3-phase frame to αβ frame

$$V_{REF} = V_A + V_B e^{j120} + V_C e^{j240} \tag{6.12}$$

$$V_{REF} = V_A + V_B(\cos 120 + j \sin 120) + V_C(\cos 240 + j \sin 240) \tag{6.13}$$

$$V_{REF} = V_A + V_B \cos 120 + V_C \cos 240 + j(\cos 120 + j \sin 120) + V_C(\cos 240 + j \sin 240) \tag{6.13}$$

$$V_{REF} = V_A + V_B \cos 120 + V_C \cos 240 + j(V_B \sin 120 + V_C \sin 240) \tag{6.14}$$

Hence,

$$V_{REF} = V_\alpha + jV_\beta \tag{6.15}$$

Where

$$V_\alpha = V_A - \frac{1}{2}V_B - \frac{1}{2}V_C \tag{6.16}$$

$$V_\beta = \frac{\sqrt{3}}{2}V_B - \frac{\sqrt{3}}{2}V_C \tag{6.17}$$

Hence, the Clark transformation can be written as

$$\begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} = \begin{pmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{pmatrix} \begin{pmatrix} V_{AO} \\ V_{BO} \\ V_{CO} \end{pmatrix} \tag{6.18}$$

The Park transformation can be performed by rotating the αß frame by an angle (θ) resulting in the dq frame as shown in Fig. 6.7 below. Mathematically, the resulting V_d and V_q components can be expressed as

$$V_q = V_{REF} \sin(\gamma - \theta) \tag{6.19}$$

$$V_d = V_{REF} \cos(\gamma - \theta) \tag{6.20}$$

Expanding using trigonometric yields

$$V_q = V_{REF} \sin(\gamma - \theta) = V_{REF}(\sin\gamma \cos\theta - \cos\gamma \sin\theta) \tag{6.21}$$

$$V_q = V_{REF} \cos(\gamma - \theta) = V_{REF}(\cos\gamma \cos\theta + \sin\gamma \sin\theta) \tag{6.22}$$

Note that

$$\gamma = \tan^{-1}\left(\frac{V_\beta}{V_\alpha}\right) \tag{6.23}$$

$$\sin\gamma = \sin\left(\tan^{-1}\left(\frac{V_\beta}{V_\alpha}\right)\right) = \frac{V_\beta}{V_{REF}} \quad \text{and} \quad \cos\gamma = \cos\left(\tan^{-1}\left(\frac{V_\beta}{V_\alpha}\right)\right) = \frac{V_\alpha}{V_{REF}} \tag{6.24}$$

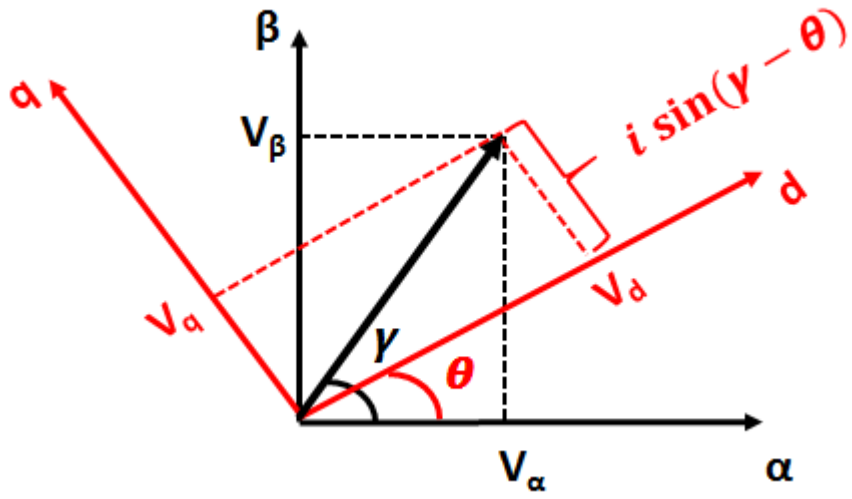


Fig. 6.7 Conversion of αß frame to dq frame

Combining equations (6.21) and (6.24) yields

$$V_q = V_{REF}\left(\sin\gamma\cos\theta - \cos\gamma\sin\theta\right) = V_\beta\cos\theta - V_\alpha\sin\theta \tag{6.25}$$

$$V_d = V_{REF}\left(\cos\gamma\cos\theta + \sin\gamma\sin\theta\right) = V_\alpha\cos\theta + V_\beta\sin\theta \tag{6.26}$$

Hence, the dq components of the voltage can be expressed as

$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = \begin{pmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{pmatrix}\begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} \tag{6.27}$$

$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = \begin{pmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{pmatrix}\begin{pmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{pmatrix}\begin{pmatrix} V_{AO} \\ V_{BO} \\ V_{CO} \end{pmatrix} \tag{6.28}$$

$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = \begin{pmatrix} \cos\theta & \frac{\sqrt{3}}{2}\sin\theta - \frac{1}{2}\cos\theta & -\frac{\sqrt{3}}{2}\sin\theta - \frac{1}{2}\cos\theta \\ -\sin\theta & \frac{1}{2}\sin\theta + \frac{\sqrt{3}}{2}\cos\theta & \frac{1}{2}\sin\theta - \frac{\sqrt{3}}{2}\cos\theta \end{pmatrix} \begin{pmatrix} V_{AO} \\ V_{BO} \\ V_{CO} \end{pmatrix} \tag{6.29}$$

$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = \begin{pmatrix} \cos\theta & \cos(\theta-120) & \cos(\theta+120) \\ -\sin\theta & \sin(\theta-120) & \sin(\theta+120) \end{pmatrix} \begin{pmatrix} V_{AO} \\ V_{BO} \\ V_{CO} \end{pmatrix} \tag{6.30}$$

To make the transformation invertible and power invariant between both reference frames, equation 6.30 can be written as

$$\begin{pmatrix} V_d \\ V_q \\ 0 \end{pmatrix} = \frac{2}{3} \begin{pmatrix} \cos\theta & \cos(\theta-120) & \cos(\theta+120) \\ -\sin\theta & \sin(\theta-120) & \sin(\theta+120) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix} \begin{pmatrix} V_{AO} \\ V_{BO} \\ V_{CO} \end{pmatrix} \tag{6.31}$$

where is a zero-sequence component is added to make the matrix square and invertible.

Each of the 27 switching states of the converter correspond to a vector in the αß frame. Table 6.3 below shows the calculated V_α and V_β for each of the 27 switching states along with the magnitude and angle of each vector. The 3 zero vectors occur when the phase voltage of the 3 phases are equal meaning all the line voltages are zero. Fig. 6.8 below shows the switching pattern of the converter for the 3 zero vectors.

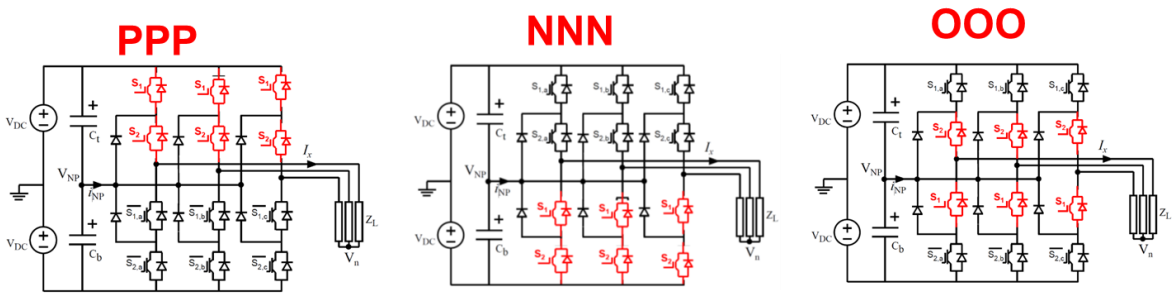


Fig. 6.8 The 3L-NPC switching states resulting in the 3 zero vectors

Table 6.3 3L-NPC Converter showing switching states with corresponding αß values

Space vector						Switching state	Load phase voltages		
Name		V_α	V_β	Magnitude	Phase angle		V_{An}	V_{Bn}	V_{Cn}
V_0		0	0	0	0	[NNN]	0	0	0
						[OOO]			
						[PPP]			
V_1	V_{1P}	$V_D/3$	0	$V_D/3$	0	[POO]	$V_D/3$	$-V_D/6$	$-V_D/6$
	V_{1N}					[ONN]			
V_2	V_{2P}	$V_D/6$	$\sqrt{3}\,V_D/6$		$\pi/3$	[PPO]	$V_D/6$	$V_D/6$	$-V_D/3$
	V_{2N}					[OON]			
V_3	V_{3P}	$-V_D/6$	$\sqrt{3}\,V_D/6$		$2\pi/3$	[OPO]	$-V_D/6$	$V_D/3$	$-V_D/6$
	V_{3N}					[NON]			
V_4	V_{4P}	$-V_D/3$	0		π	[OPP]	$-V_D/3$	$V_D/6$	$V_D/6$
	V_{4N}					[NOO]			
V_5	V_{5P}	$-V_D/6$	$-\sqrt{3}\,V_D/6$		$4\pi/3$	[OOP]	$-V_D/6$	$-V_D/6$	$V_D/3$
	V_{5N}					[NNO]			
V_6	V_{6P}	$V_D/6$	$-\sqrt{3}\,V_D/6$		$5\pi/3$	[POP]	$V_D/6$	$-V_D/3$	$V_D/6$
	V_{6N}					[ONO]			
V_7		$V_D/2$	$\sqrt{3}\,V_D/6$	$\sqrt{3}\,V_D/3$	$\pi/6$	[PON]	$V_D/2$	0	$-V_D/2$
V_8		0	$\sqrt{3}\,V_D/3$		$\pi/2$	[OPN]	0	$V_D/2$	$-V_D/2$
V_9		$-V_D/2$	$\sqrt{3}\,V_D/6$		$5\pi/6$	[NPO]	$-V_D/2$	$V_D/2$	0
V_{10}		$-V_D/2$	$-\sqrt{3}\,V_D/6$		$7\pi/6$	[NOP]	$-V_D/2$	0	$V_D/2$
V_{11}		0	$-\sqrt{3}\,V_D/3$		$3\pi/2$	[ONP]	0	$-V_D/2$	$V_D/2$
V_{12}		$V_D/2$	$-\sqrt{3}\,V_D/6$		$11\pi/6$	[PNO]	$V_D/2$	$-V_D/2$	0
V_{13}		$2V_D/3$	0	$2V_D/3$	0	[PNN]	$2V_D/3$	$-V_D/3$	$-V_D/3$
V_{14}		$V_D/3$	$\sqrt{3}\,V_D/3$		$\pi/3$	[PPN]	$V_D/3$	$V_D/3$	$-2V_D/3$
V_{15}		$-V_D/3$	$\sqrt{3}\,V_D/3$		$2\pi/3$	[NPN]	$-V_D/3$	$2V_D/3$	$-V_D/3$
V_{16}		$-2V_D/3$	0		π	[NPP]	$-2V_D/3$	$V_D/3$	$V_D/3$
V_{17}		$-V_D/3$	$-\sqrt{3}\,V_D/3$		$4\pi/3$	[NNP]	$-V_D/3$	$-V_D/3$	$2V_D/3$
V_{18}		$V_D/3$	$-\sqrt{3}\,V_D/3$		$5\pi/3$	[PNP]	$V_D/3$	$-2V_D/3$	$V_D/3$

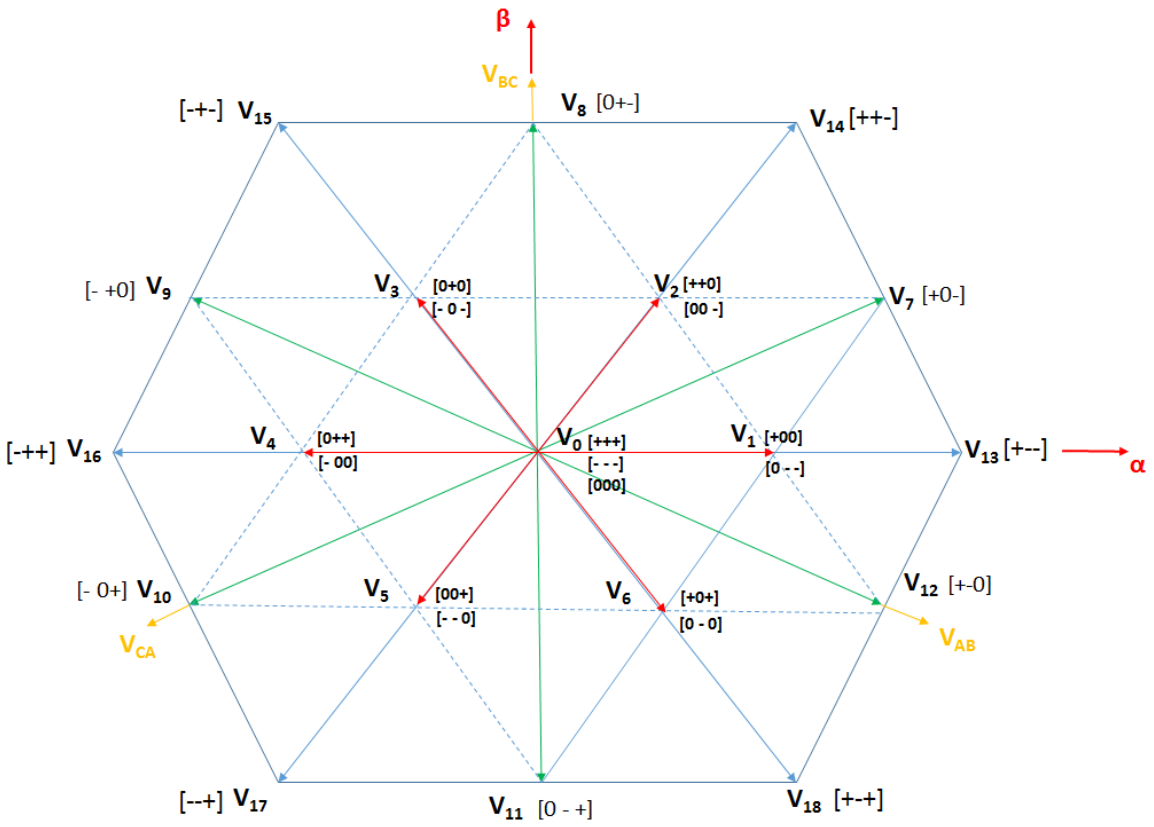


Fig. 6.9 3L-NPC Converter switching vector diagram in αß frame

Looking at table 6.3, there 3 zero vectors (with magnitude 0), 12 short vectors (with magnitude $V_{DC}/3$), 6 medium vectors (with magnitude $\sqrt{3}V_{DC}/3$) and 6 long vectors (with magnitude $2V_{DC}/3$). It is interesting to note that each small vector has 2 switching states that result in the exact same vector magnitude and phase angle. The asymmetry in the application of these vectors can cause neutral point drift resulting in unequal capacitor voltage which can have destructive consequences if left uncontrolled. Neutral point drift is due to a non-zero average neutral point current causes a divergence in capacitor voltage. In the next section of the thesis, the control principles developed here are used

in the simulation of a permanent magnetic synchronous machine driven by an NPC converter.

6.3 AC Motor Drive Simulations

This section describes the electro-thermal model for the AC motor drive using an NPC converter. The AC drive model is implemented in MATLAB/Simulink and it is comprised of electrical, thermal and control sub-systems. The electrical model consists an ideal voltage source (battery), DC-link capacitors with a neutral point, a 3 level NPC inverter and a 3-phase permanent magnet synchronous motor. Fig. 6.10 shows the schematic of the power electronic side of the AC drive consisting a voltage source, inverter and the PMSM.

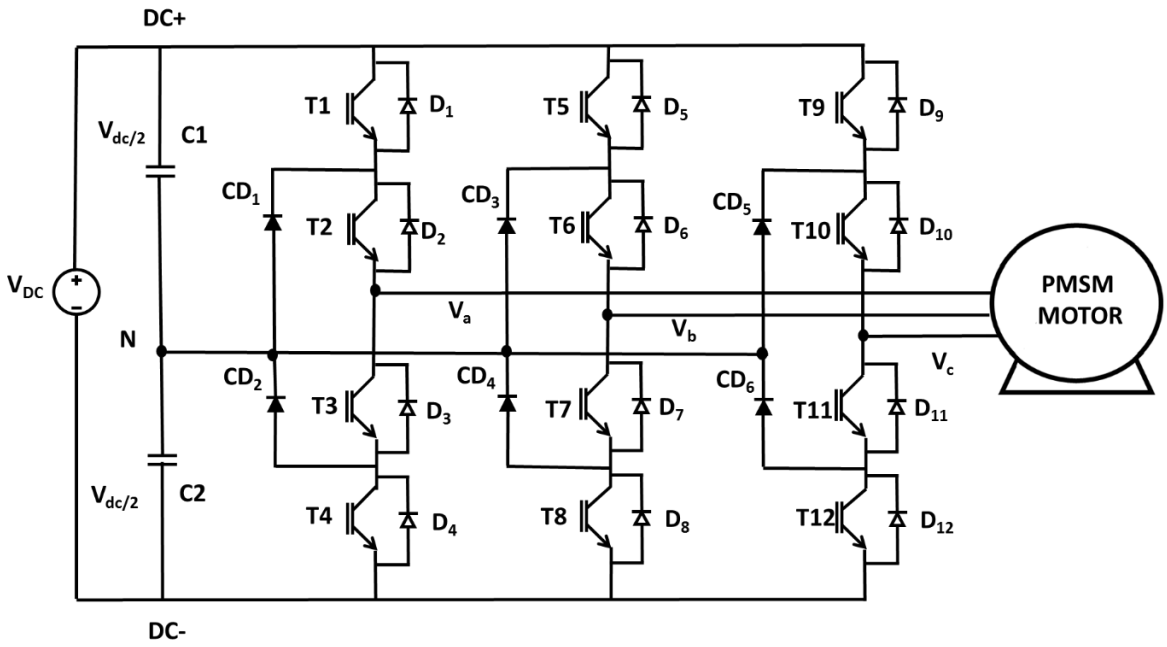


Fig. 6.10 The schematic of the three-phase three-level NPC inverter.

The control of the PMSM is a field oriented control which controls the d-q components of the current to deliver the desirable torque [21-22, 26]. The electro-thermal model works simultaneously with the electrical model and it calculates the conduction and switching losses of each device in the 3-level NPC inverter using the lookup table of losses for turn-on and turn-off and calculates the conduction losses based on the forward characteristic of the device obtained from the datasheet. The losses are fed to a Cauer-thermal network of each device and the junction temperature of each device is calculated. The junction temperatures are used as a feedback to calculate accurate losses for the next step of the simulation [23-25]. Fig. 6.11 shows a high level block diagram of the complete model.

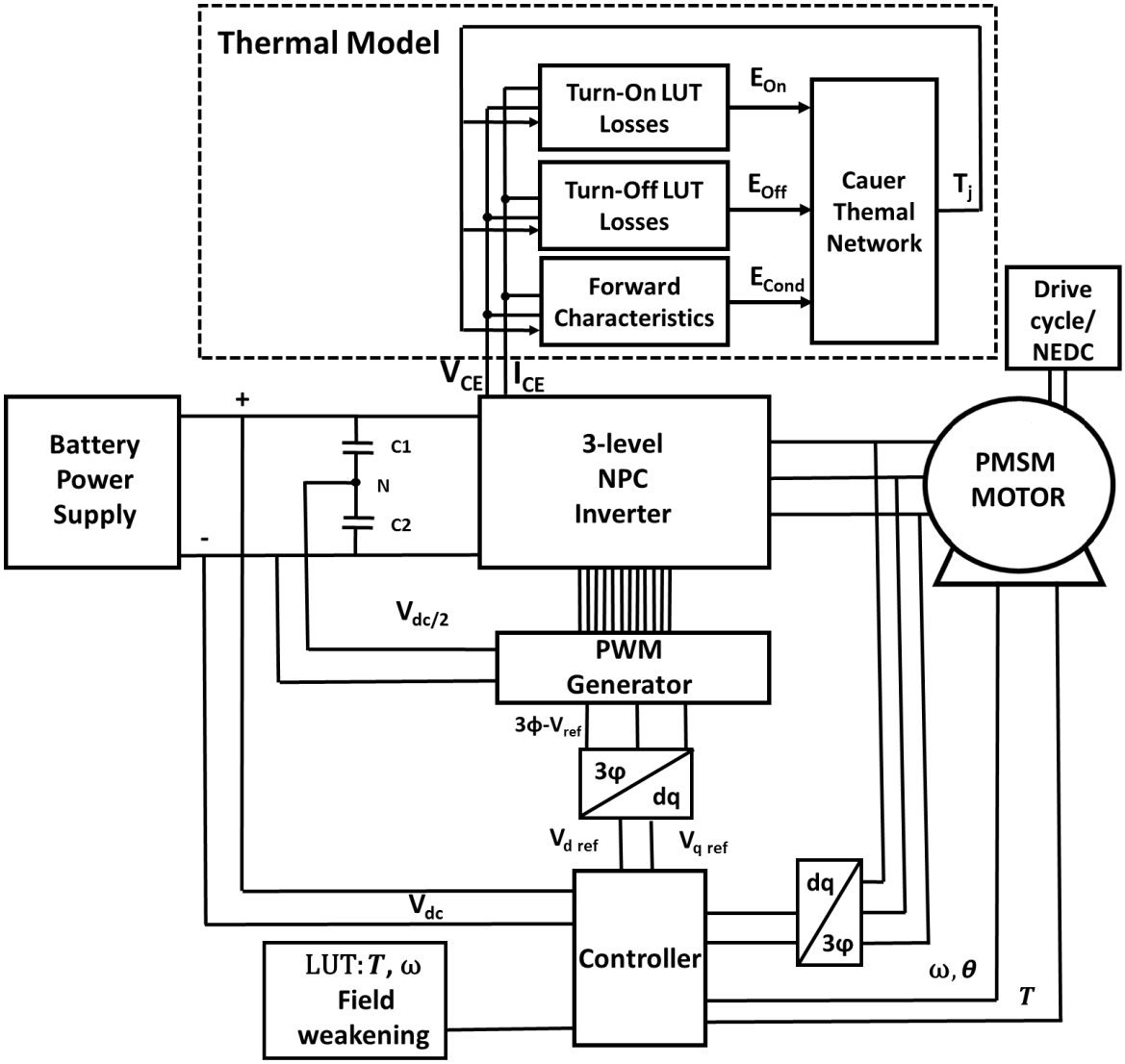


Fig. 6.11 Top level overview of the electro-thermal model of the AC drive.

6.3.1 Drive Model Development

The controller uses the absolute rotor position (usually obtained from a resolver), three phase currents and torque as input and provides three phase voltage references. Fig. 6.11 shows the block diagram of the controller.

The PMSM torque is sum of mutual torque and cogging torque:

$$T_e = T_{em} + T_{ec} \tag{6.32}$$

The mutual torque is calculated using instant values of phase currents and back EMF. The cogging torque is due to the energy in the magnetic field due to the rotor permanent magnets in open circuit configuration [27, 28].

$$T_{em} = \frac{I_d V_d + I_q V_q}{\omega_m} \tag{6.33}$$

$$T_{ec} = -\frac{dE_0(\theta_m)}{d\theta_m} \tag{6.34}$$

Hence, the equation relating the I_q component of the stator current and the torque is achieved:

$$T_{em} = \frac{3}{2} p \lambda_f I_q \tag{6.35}$$

In this equation λ_f is the maximal flux linkage due to the permanent magnets of the rotor and p is the number of pole pairs. Based on this equation, a PI controller can be

used to obtain the I_q reference current using the error between the requested torque and the measured torque.

I_d is usually kept to be zero as it does not contribute in generating torque and it is in form of reactive power. The back EMF generated at the stator windings are proportional to the speed of the motor. At high speeds, the generated back EMF becomes significantly larger up to a point where the phase voltage required to generate the torque becomes greater than the maximum allowed voltage from the voltage source. Hence, the electric machine cannot deliver the expected torque. At such conditions, a negative I_d current in form of a reactive power is injected to the windings to weaken the flux due to the permanent magnets. This is known as field weakening [26]. In this model a flux weakening map is used to provide the reference I_d at high speeds. The phasor diagram showing the field weakening concept is shown in Fig. 6.12.

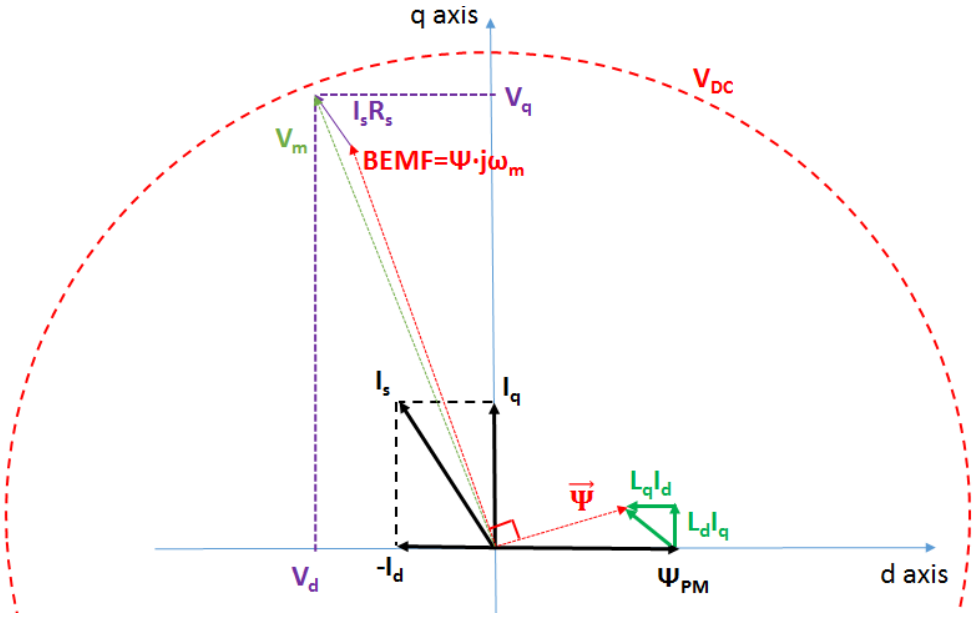


Fig. 6.12 Field weakening concept

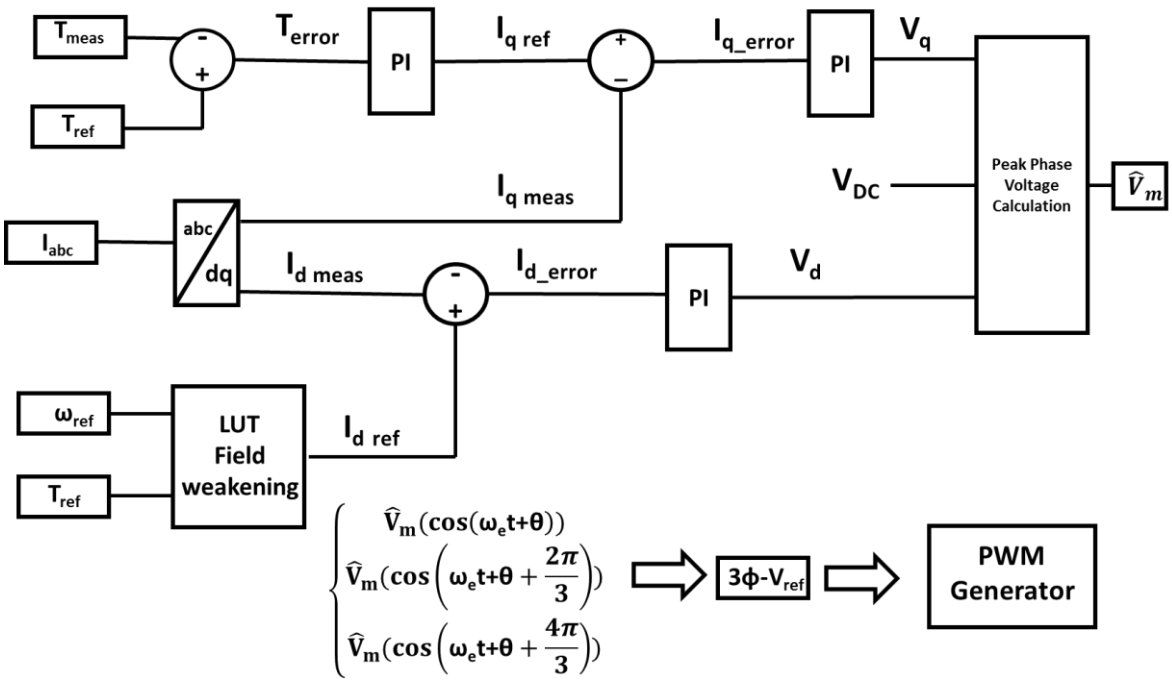


Fig. 6.13 Current controller

In order to control the current, feedback currents from the three phases of the motor are used to get the d-q components of the currents. These currents are compared to the reference I_d and I_q currents. The PI controllers used to obtain the reference voltages are based on the d-q voltage equations of the PMSM.

$$V_d = R_S I_d + L_d \frac{dI_d}{dt} - pw_m I_q L_q \tag{6.36}$$

$$V_q = R_S I_q + L_q \frac{dI_q}{dt} + pw_m (I_d L_d + \psi_m) \tag{6.37}$$

Fig. 6.13 shows the block diagram of the current control and the reference voltage generator.

The three phase voltage references (3φ-V_{ref}) obtained from the block diagram above are fed to the SPWM gate signal generator.

In this model, a flux-weakening map is used to provide the reference I_d at high speeds. This signal generator uses the three-level neutral point voltage balance control scheme based on carrier overlapping SPWM method to balance the DC link capacitor voltages [29].

In previous works [30, 31], the temperature imbalance between the IGBTs used in the grid connected 3-level NPC was investigated and it was shown that the temperature of the top device is higher than the temperature of the middle devices in a leg of the inverter. However, in a drive application, this is not the case. When the motor is operating in a drive cycle, when the motor accelerates and the speed increases the

inverter is operating in the first quadrant and torque is positive. In contrast, when the motor decelerates it is working in the regenerative mode and torque is negative. During these different operation points, the stress distribution on the devices are different as the current path is different. Moreover, during the field weakening, when a reactive power is absorbed from the motor, the stress distribution changes.

6.3.2 Thermal Model for Power Devices

Lumped RC Cauer-thermal networks are used to model the junction temperature rise of each device due to the conduction and switching losses. The reason for choosing this type of equivalent circuit is that it can be derived from the device's physical dimensions and material properties. The thermal model is based on two assumptions. Firstly, the heat flow is unidirectional– i.e. the heat flux propagates in one direction from the chip junction down to the base plate and heat sink. Secondly, there is no significant thermal coupling between different semiconductor chips; i.e. no lateral heat flow between chips within the same module.

This simplified thermal model is accurate enough for the purposes of this research. Laboratory experiments on the same power module and heat sink from which the thermal model was derived have shown that the water-cooling system draws the heat efficiently away from the junction with relatively small thermal time constant. This minimizes the lateral heat spread and temperature rise that can be observed in air-cooled heat sinks. The module used for the purposes of the simulation is the

Semikron half-bridge module SKM50GB12T4 with rated current of 50A and DC voltage of 1200V. Fig.6.14 illustrates the internal layout of its DBC with a focus on the IGBT chip.

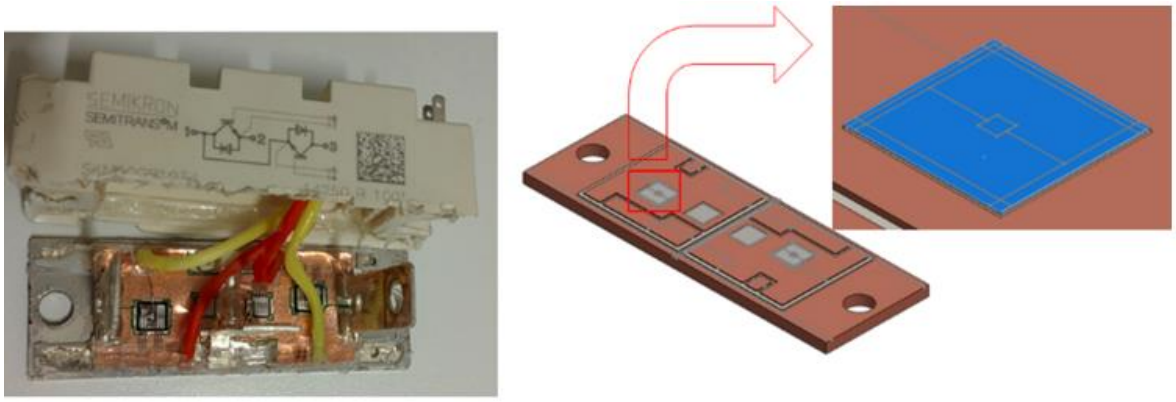


Fig. 6.14 SKM50GB12T4 half-bridge IGBT module with two IGBT and two free-wheeling diodes.

Each Cauer ladder contains nine R_{th} C_{th} steps – one for each material layer in the multilayer cross-section of the module including the thermal interface and the heat sink. The different layers of this network are shown in Fig. 6.15. A module was specifically disassembled to study its structure and chip dimensions which were used in the parameter extraction for the Cauer ladder. Fig. 6.15 illustrates all layers considered (not to scale) and the Cauer network with all its corresponding R_{th} and C_{th} values. The thermal capacitances are calculated from the material's volumetric specific heat capacity (s) and the volume of each corresponding layer (V):

$$C_{th} = s \cdot V \tag{6.38}$$

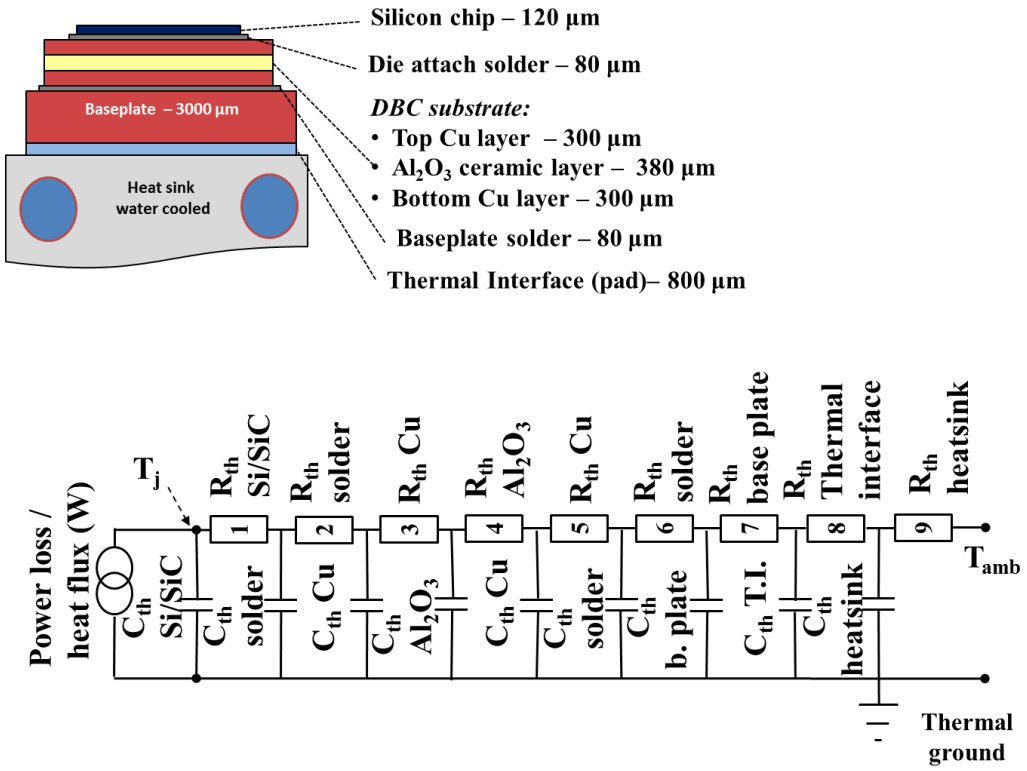


Fig. 6.15 Cross-sectional view of power semiconductor device and the corresponding Cauer-network of the device

The thermal resistances are calculated across the two adjacent layers, from the centre of one to the centre of the other. As shown in Fig. 6.16, this results in obtaining the temperature of the layer itself rather than the interface between two layers. Hence, the most representative physical position of such temperature measurement will be midway through the layer. The R_{th} is thus the combined thermal resistance of the bottom half of the first layer and top half of the following layer calculated using layer dimensions (thickness and area) and the material heat conductivity value (k) [32]:

$$R_{th} = \frac{d_1}{2k_1A_1} + \frac{d_2}{2k_2A_2} \tag{6.39}$$

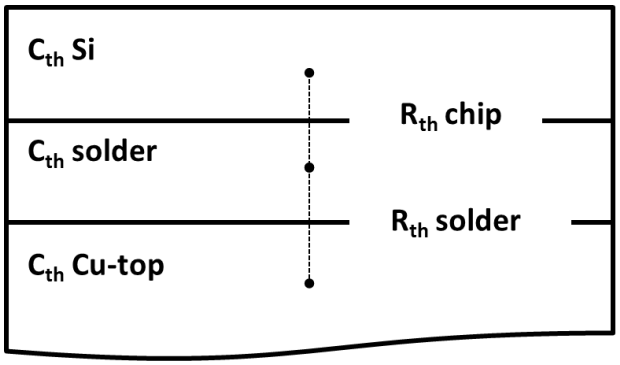


Fig. 6.16 The different material layers with internal capacitances and resistances between the layers

Table 6.4 contains the extracted R_{th} and C_{th} values for the above discussed IGBT module with Silicon chips and a hypothetical module of the same dimensions but using a SiC chip from *Wolfspeed* (CPM2-1200-0025B). The simulations of the converter losses and thermal behavior have been performed for both cases using the same core thermal Cauer ladders with updated branch values.

Table 6.4 Cauer network R_{th} and C_{th} values used in the electro-thermal simulation

	Layer	R_{th} Si (K/W)	C_{th} Si (Ws/K)	R_{th} SiC (K/W)	C_{th} SiC (Ws/K)
1	Chip	2.18×10^{-2}	1.005×10^{-2}	3.019×10^{-2}	1.037×10^{-2}
2	Solder	1.296×10^{-2}	7.118×10^{-3}	2.419×10^{-2}	3.476×10^{-3}
3	Cu-top	1.151×10^{-2}	1.734×10^{-1}	1.151×10^{-2}	1.734×10^{-1}
4	Al_2O_3	9.779×10^{-3}	9.817×10^{-1}	9.779×10^{-3}	9.817×10^{-1}
5	Cu-bottom	1.281×10^{-3}	7.605×10^{-1}	1.281×10^{-3}	7.605×10^{-1}
6	Solder	2.111×10^{-3}	9.899×10^{-1}	2.111×10^{-3}	9.899×10^{-1}
7	Cu base plate	8.011×10^{-2}	28.952	8.011×10^{-2}	28.952
8	Thermal pad	7.969×10^{-2}	2.7081	7.969×10^{-2}	2.7081
9	Heat sink	9.254×10^{-4}	1460.154	9.254×10^{-4}	1460.154

The losses injected into the thermal network is calculated using 3-D lookup table (LUT) of losses for conduction, switch-on and switch-off. The dimensions are current, voltage and temperature. Transistors and clamping diodes and freewheeling diodes have separate LUT of losses. The data for these LUT of losses are obtained from the device datasheet. The process of calculating the switching losses starts from detecting the switching for all the devices. Hence, for each device a logic circuit is used to detect the switch-ON and switch-OFF and based on the junction temperature, the voltage and the current of each device, the switching loss for each device throughout the mission profile is calculated. The conduction losses of each device are calculated from the forward characteristic LUT at different temperatures which provides the on-state resistance of the device by taking the temperature, voltage and current of each device. The on-state resistance and current passing through the device is used to obtain the power loss and the energy loss under the operation of the device. Fig. 6.17 illustrates this process using a simplified block diagram.

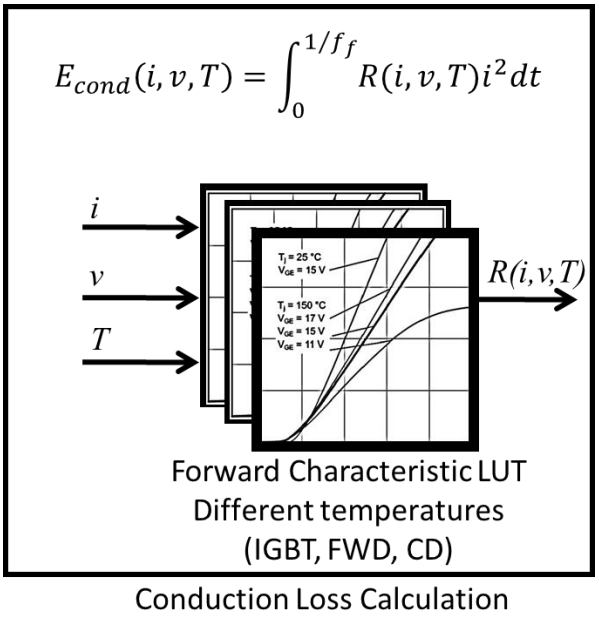


Fig. 6.17 Block diagram of conduction loss calculation

The sum of conduction and switching losses of each device is fed to the Cauer thermal network of each device and the junction temperature is calculated by the end of each time step. The model is compatible with any mission profile.

6.3.3 Results and Discussions

The New European Driving Cycle (NEDC) was used as the mission profile. The drive cycle was designed to assess the emission level of cars. Based on this drive cycle, the target torque and speed of the PMSM is calculated and the full mission profile for 10 minutes of operation is shown in Fig. 6.18. More specifically, in order to analyze the loss distribution within the 3L-NPC inverter under the inverter motoring mode, the flux-weakening mode and the regenerative mode, the time period between 300 and 400

seconds of the mission profile is chosen for further scrutiny. During this period of time in the NEDC drive cycle, the electric motor accelerates in motor mode and the torque reaches the maximum value after which the electric motor starts decelerating and the motor goes to regenerative brake mode and acts as a generator. Moreover, due to the high torque request at high speed, a negative I_d current is also injected during this period of time in the cycle thereby causing the power factor of the motor to decrease and putting more electrothermal stress on the inner transistors (T2 and T3).

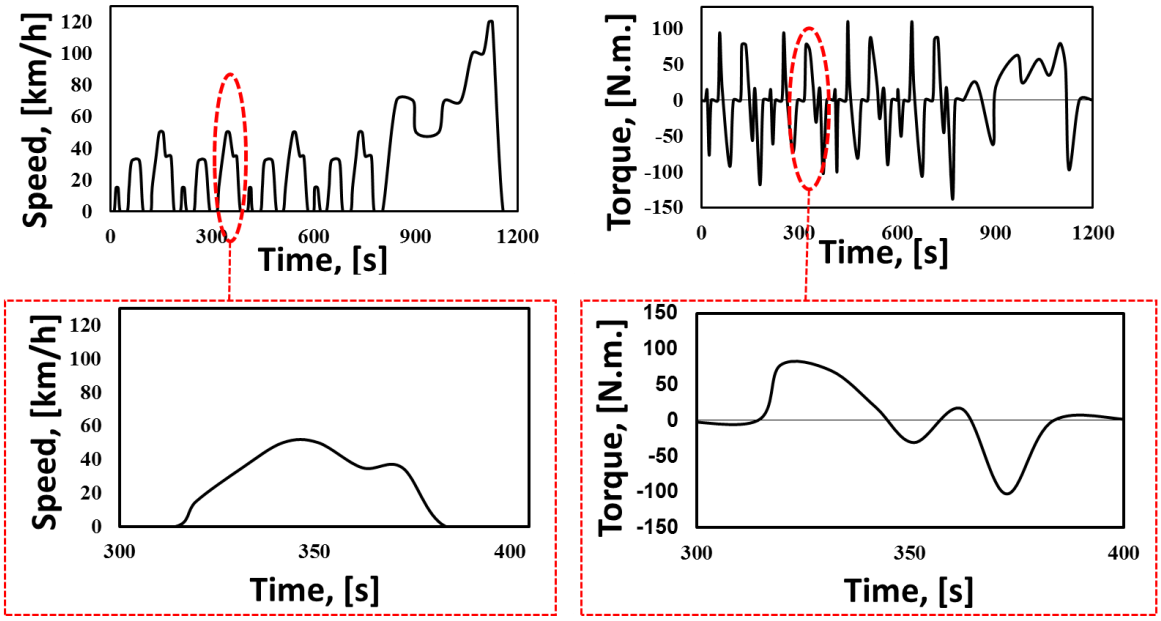


Fig. 6.18 Speed and Torque of NEDC drive cycle

Fig. 6.19 shows the junction temperature rise within T1 and T2 in the silicon IGBT-based power inverter between 300 and 400 seconds in the drive cycle. The drive cycle goes through a motoring phase, a flux-weakening phase and a regenerative braking

phase. During this period, the 3L-NPC converter is inverting during the motoring phase, it is absorbing reactive power during the flux-weakening phase and it is rectifying during the regenerative braking phase. As can be seen from Fig. 15, the temperature of T2 is higher than the temperature of the T1 and this is more significant when the motor goes to the flux-weakening mode as T2 conducts more during this period and consequently, the temperature of this transistor is higher.

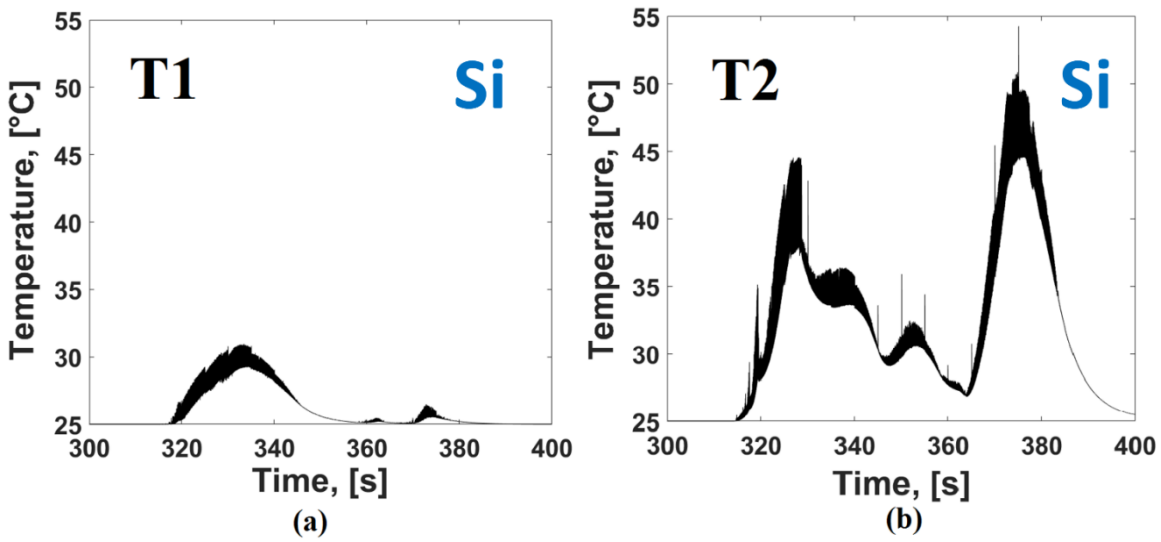


Fig. 6.19 Temperature rise of Si IGBT devices in the 3L-NPC inverter between 300 and 400 seconds: (a) T1, (b) T2.

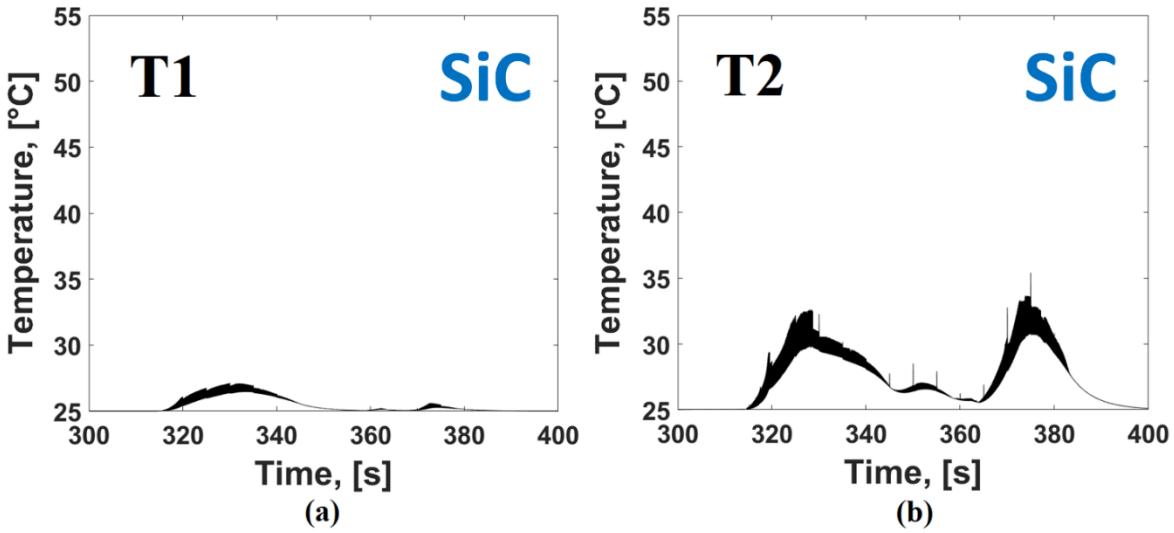


Fig. 6.20 Temperature rise of SiC MOSFET devices in the 3L-NPC inverter between 300 and 400 seconds: (a) T1, (b) T2.

Fig. 6.20 shows the comparison of temperature rise for the SiC-based power 3L-NPC inverter. Comparing this graph with the results shown in Fig. 6.19, it can be seen that there is a similar trend in the temperature rise of T1 and T2; however, the temperature rise for both devices are smaller compared to the Si IGBT based 3L-NPC inverter. It can be observed that for both simulated inverters, the thermal stress on T2 is higher than T1 during the flux-weakening phase of the drive cycle mission profile. This is due to the fact that the converter is absorbing reactive power from the machine during flux weakening, hence, there is considerable phase lag between the current and the voltage. As a result, the peak current occurs during small and medium voltage vectors where the inner transistors (T2 and T3) and the clamping diodes are more active. This observation is similar to that made in [31] where the 3L-NPC converter loss distribution was analysed for a grid connected inverter under low voltage ride through (LVRT) conditions. Under these conditions, the inverter is expected to supply

reactive power to the grid in order to support the grid voltage during AC side faults. It was observed that under these conditions, the inner transistors (T2 and T3) and the clamping diodes were more electrothermally stressed than the outer transistors (T1 and T4). Hence, under the flux-weakening mode in the electric drive cycle, the 3L-NPC exhibits a similar loss distribution between the devices as it would under LVRT conditions.

Fig. 6.21 shows the total power losses of T1 and T2 in Si-IGBT based 3L-NPC converter, whereas Fig. 6.22 shows the same losses for the SiC based converter. As can be observed, the losses of Si-IGBT devices (T1 and T2) are twice the losses of SiC-based devices. This is due to the considerably lower switching losses of SiC MOSFETs compared to Si-IGBTs due to the absence of stored charge that must be removed by long tail currents and reverse recovery charge in the case of PiN diodes.

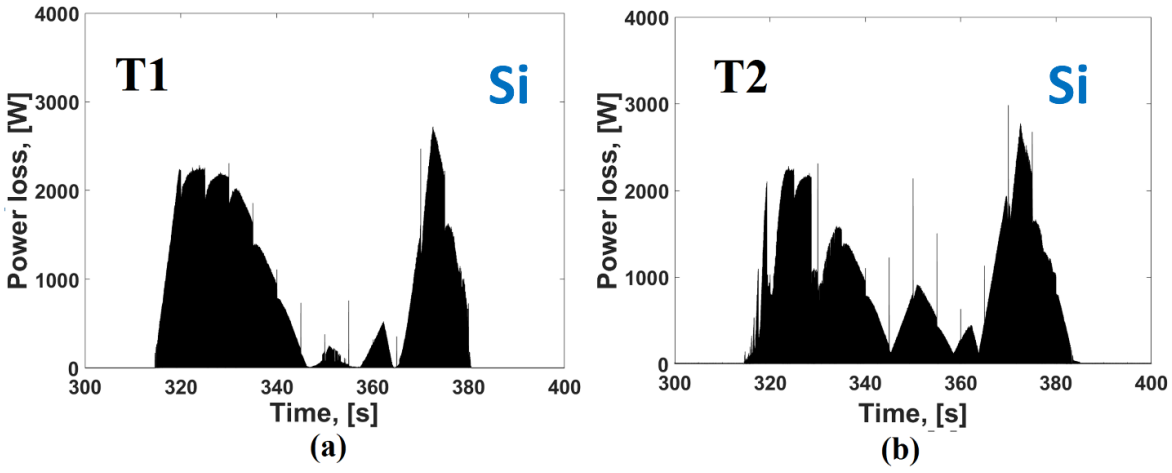


Fig. 6.21 Total power loss of Si IGBT devices in the 3L-NPC inverter between 300 and 400 seconds: (a) T1, (b) T2.

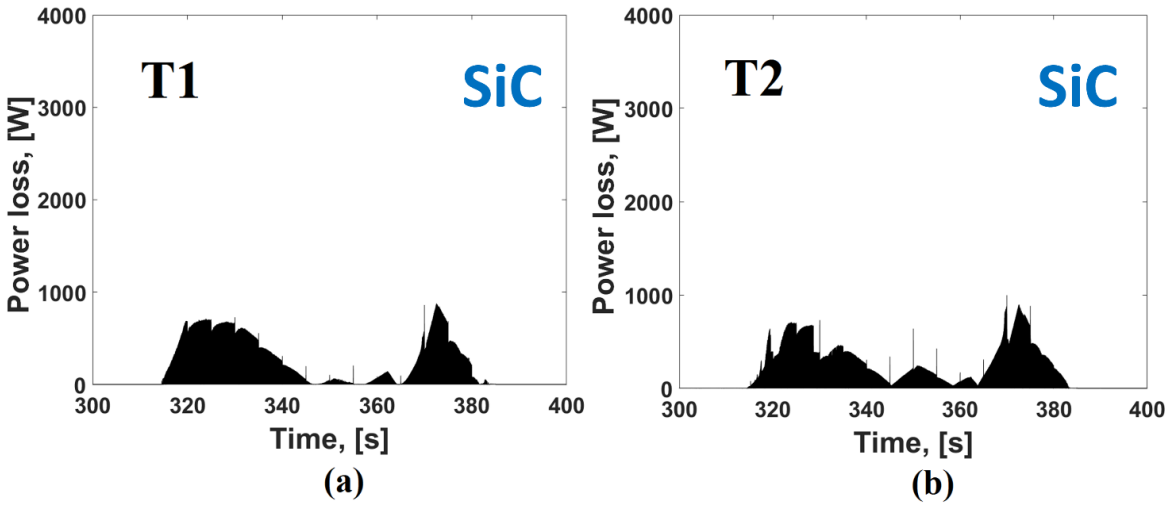


Fig. 6.22 Total power loss of SiC MOSFET devices in the 3L-NPC inverter between 300 and 400 seconds: (a) T1, (b) T2.

The simulated power losses of the clamping diodes have also been extracted from the simulator. Fig. 6.23 shows the total loss of the clamping diode in the Si-IGBT 3L-NPC inverter where PiN diodes are used as the clamping diodes. The electrical simulations reveal that the switching losses of the clamping diodes are significantly higher than the conduction losses, hence, changing the clamping diodes from Si PiN diodes to SiC Schottky diodes has a significant impact on the total losses of the inverter. Fig. 6.24 shows the total losses for the SiC Schottky diodes used as clamping diodes where it can be seen that there are significantly reduced power losses.

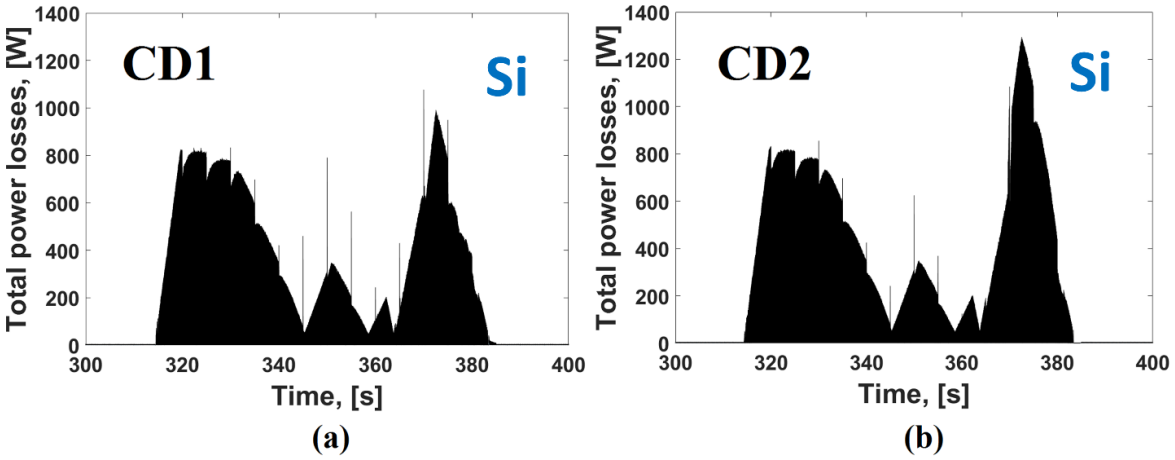


Fig. 6.23 Power losses of the Si PiN diodes as clamped diodes during drive cycle for (a) CD1 and (b) CD2.

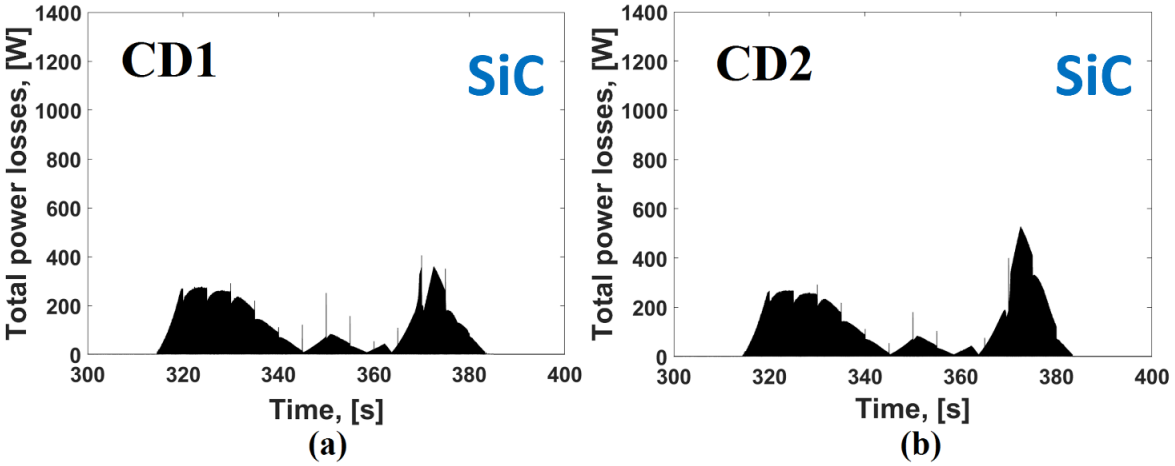


Fig. 6.24 Power losses of the SiC Schottky diodes as clamped diodes during drive cycle for (a) CD1 and (b) CD2.

Furthermore, the power losses of the freewheeling diodes in both the Si-IGBT based and SiC MOSFET based 3L-NPC inverters have been extracted from the simulation and compared in Fig. 6.25 and Fig. 6.26. As shown in these figures, the losses of freewheeling diodes in both configurations are smaller than the losses of the clamping

diodes. It can also be seen that the loss profile in both the inner (FWD2) and outer (FWD1) diodes are identical. More improvement in the efficiency of the inverter may be achieved by upgrading the clamping diode of Si-IGBT based 3L-NPC inverter into SiC Schottky diodes.

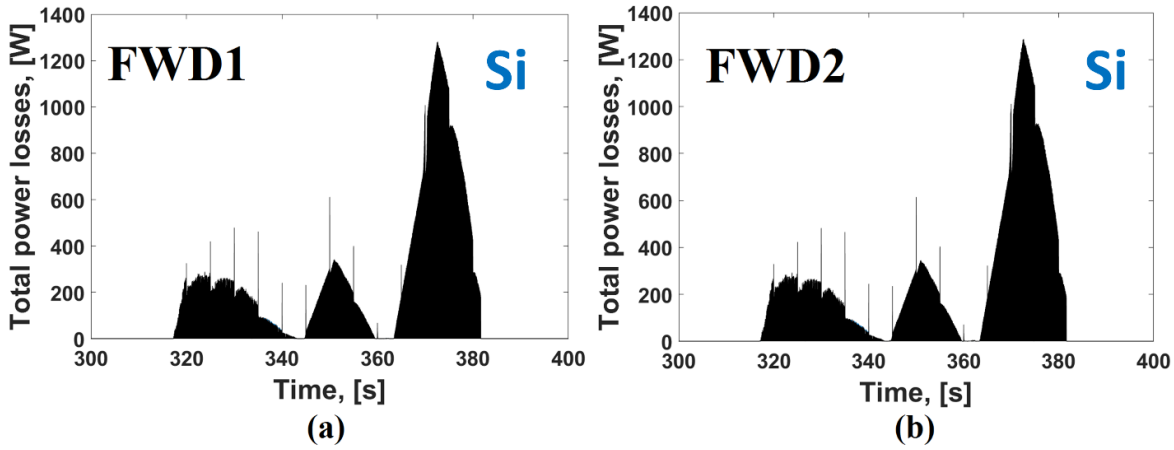


Fig. 6.25 Power losses of the Si PiN diodes as freewheeling diodes during drive cycle for (a) FWD1 and (b) FWD2.

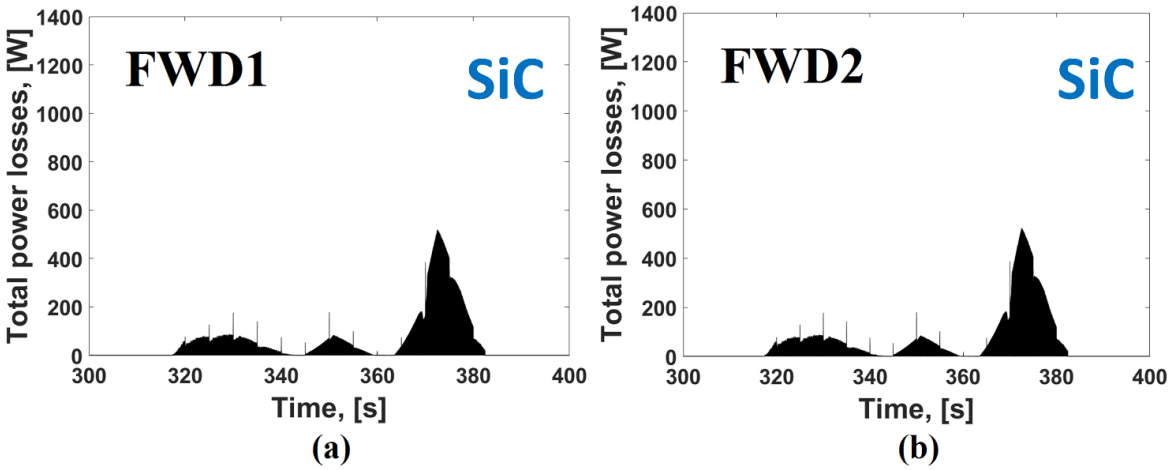
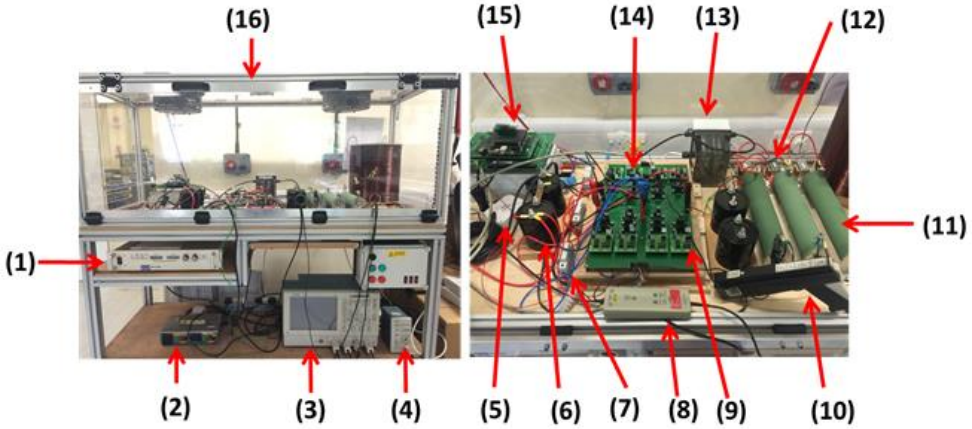
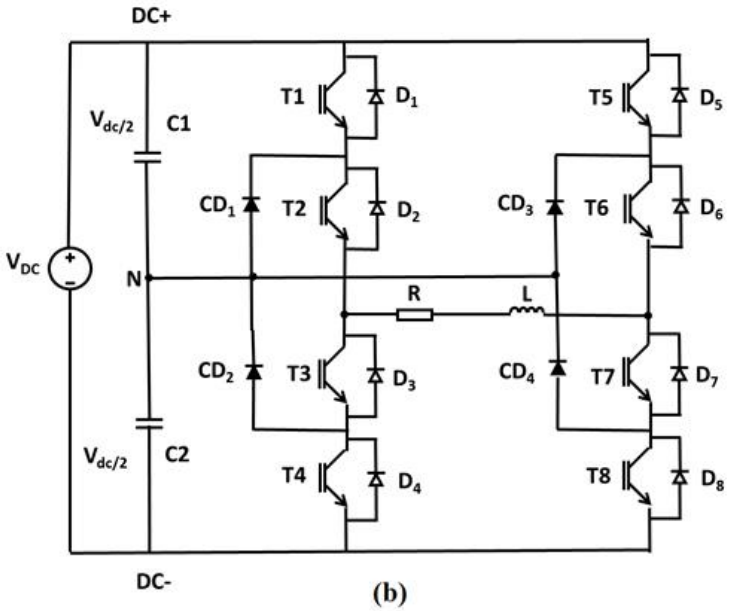


Fig. 6.26 Power losses of the SiC Schottky diodes as freewheeling diodes during drive cycle for (a) FWD1 and (b) FWD2.

6.4 Experimental Set-up of 3 Level NPC Converter and Results



(a)



(b)

Fig. 6.27 (a) Experimental Test-rig setup (b) Circuit schematic of H-bridge 3-level NPC inverter.

Fig.6.27 shows the 3-level NPC H-bridge test rig designed to capture the output voltage and current. The numbering labels in this figure are the following: (1) DC Power Supply. (2) PID controller. (3) Oscilloscope. (4) Current probe Amplifier. (5) Rectifying diode. (6) DC link capacitor. (7) Fuse. (8) Differential voltage probe (9) Gate drivers (10) Current Probe. (11) Resistive load. (12) Inductive load. (13) Logic supply. (14) Power devices on break out board. (15) FPGA. (16) Test chamber.

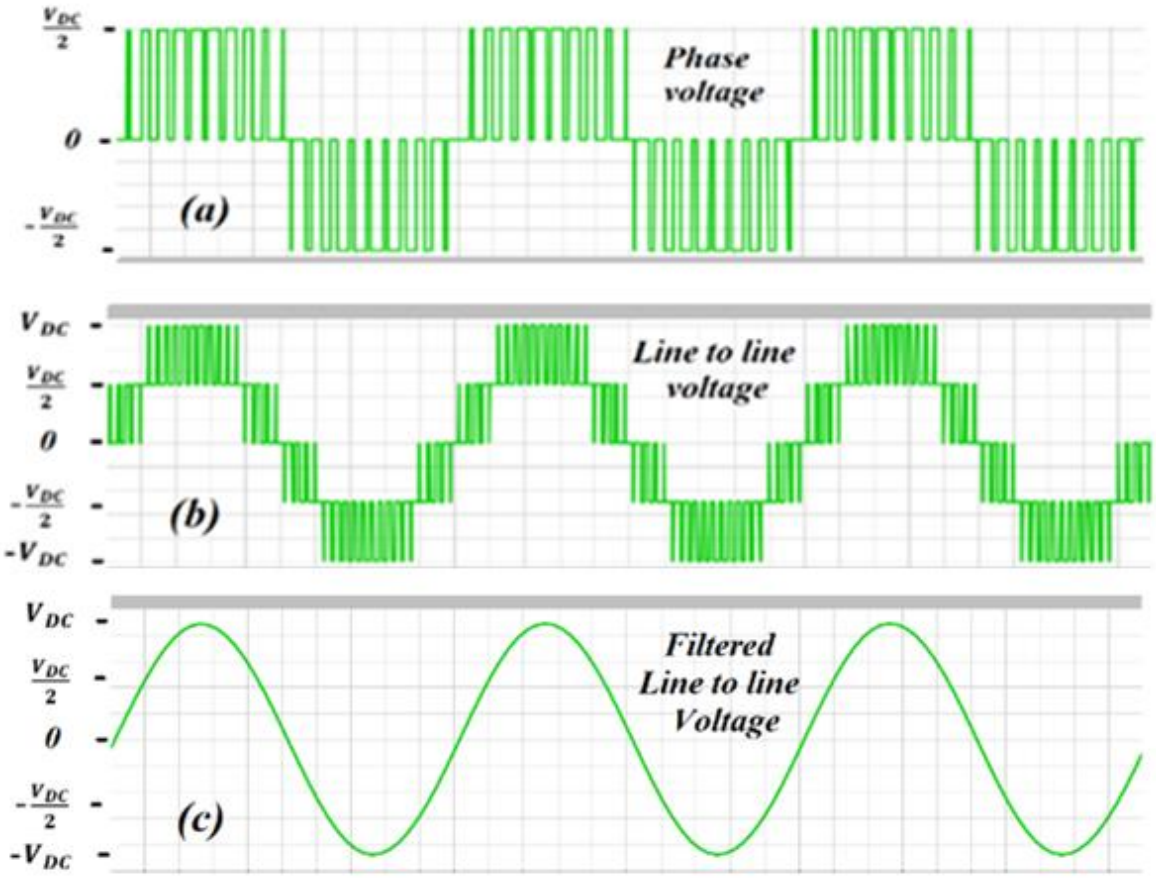


Fig. 6.28 (a) phase voltage (b) Line-to-line voltage and (c) filtered line-to-line voltage of the 3-level single phase NPC Converter

The converter has been designed using discrete transistors in TO-247 packages and clamping diodes in TO-220 packages. The SiC MOSFETs are 1.2 kV devices from ROHM with internally integrated body diodes and datasheet reference SCT2450KE. The silicon IGBTs are 1.2 kV International Rectifier devices with datasheet reference IRG4PH20KD. A load resistance of 333 Ω is used together with an LC filter. The generated converter phase voltage is shown in Fig. 6.28 (a), the generated line voltage is shown in Fig. 6.28 (b) and the filtered line voltage is shown in Fig. 6.28 (c). The converter DC side voltage is 500 V and the load power factor under these conditions is 1.

Four different semiconductor platforms were chosen for efficiency and power loss evaluation of 3-level NPC inverter. Platform 1 uses Si- IGBTs with silicon PiN diodes as freewheeling diodes (FWDs) and clamping diodes (CDs). Platform 2 uses Si-IGBTs with SiC Schottky barrier diodes as FWD and CDs. Platform 3 uses Si IGBTs with silicon PiN diodes as FWDs and SiC Schottky barrier diodes as CDs. Platform 4 uses SiC MOSFETs with body diodes as FWDs and SiC Schottky diodes as CDs. The measurements have been made at unity power factor and PF=0.6 and with a supply voltage of 500 V. Figure 6.29 (a) and (b) show the impact of different gate resistances with different technologies on the inverter efficiency at unity power factor for different temperatures at 25°C and 100°C respectively.

The efficiency of the converter has been measured with the transistors switching with different gate resistances at 5 kHz switching frequencies.

As can be seen from the results in Fig. 6.29 (a) and (b), that the highest efficiency is exhibited by platform 4 where SiC MOSFETs with body diodes as anti-parallel diodes and SiC Schottky diodes as clamping diodes are used. The least efficiency is exhibited by the silicon IGBTs and PiN diodes (platform 1). As the temperature increases, the improvement of the SiC MOSFET/SBD inverter over the Si IGBT/PiN diode inverter increases presumably because of the small temperature sensitivity of SiC devices.

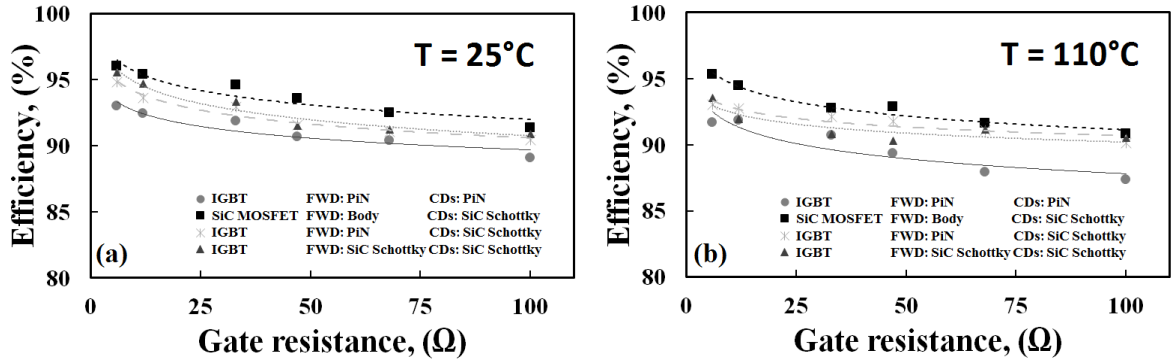


Fig. 6.29 The measured efficiency of the single phase 3 level NPC converter at PF=1 and Fs=5kHz with the different technology combinations at (a) T=25°C (b) T=110°C.

The same measurements have been performed at power factor equals 0.6. At reduced power factor the free-wheeling diodes start actively working. Figure 6.30 (a) and (b) show the impact of different gate resistances with different technologies on the inverter efficiency at PF=0.6 for different temperatures at 25°C and 100°C respectively.

The impact of the switching frequency on the conversion efficiency of the inverter has been assessed for the different technology combinations. Fig. 6.31 shows the converter efficiency as a function of the gate resistance at 5 kHz and 10 kHz for (a) the SiC MOSFET/SBD (platform 4) and (b) Si-IGBT/PiN diode (platform 1). In the case of platform 4 in Fig. 6.31 (a), it can be seen that increasing the switching frequency

increases the converter efficiency at high switching rates. For all other technology combinations, increasing the switching frequency reduces the converter efficiency. This is due to the unique switching capability of SiC diodes and MOSFETs.

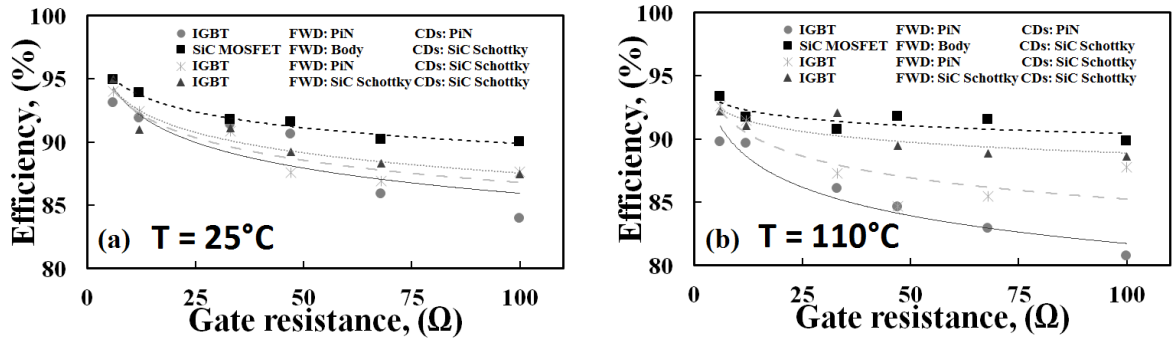


Fig. 6.30 The measured efficiency of the single phase 3 level NPC converter at PF=0.6 and Fs=5kHz with the different technology combinations at (a) T=25°C (b)T=110°C.

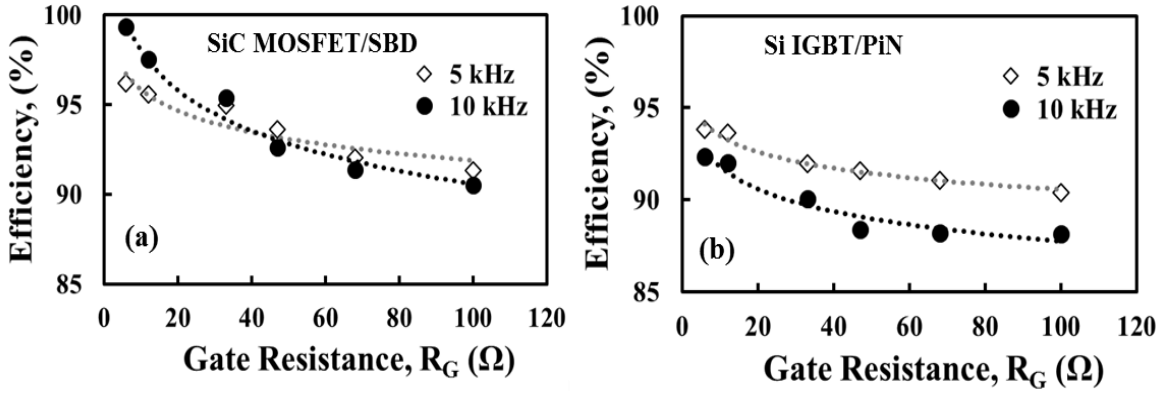


Fig. 6.31The converter efficiency as a function of gate resistance at 5 kHz and 10 kHz for (a) SiC MOSFET with SiC SBD and (b) silicon IGBT with PiN diodes.

It is clear from Fig. 6.31 (a) and Fig. 6.31 (b) that the SiC converter is more energy efficient since it exhibits lower losses. As the switching frequency is increased to 10 kHz, the efficiency of the IGBT based converter decreases further due to the poorer switching performances of silicon IGBTs compared to SiC MOSFETs.

To understand the internal distribution of these losses between the converter's components the analytical calculation of power loss distribution have been performed. Using analytical equations, the average conduction losses of the transistor was calculated as [33, 34]:

$$P_{condT} = \frac{1}{T_{sw}} \int_0^{T_{sw}} \left(V_{ce0} \cdot i_c(t) + r_c \cdot i_c^2(t) \right) dt \tag{6.40}$$

Where V_{ce0} - on-state zero-current collector-emitter voltage, r_c – collector-emitter on-state resistance.

The switching losses of the transistor was calculated as:

$$P_{swT} = \left(E_{on} + E_{off} \right) \cdot f_{sw} \tag{6.41}$$

Where E_{on} – turn-on energy of the transistor, E_{off} - turn-off energy of the transistor.

The loss distribution has been analysed for two different power factors (PF=1 and PF=0.6) at full power rating with a switching frequency of 5 kHz. Fig. 6.32 (a) shows the loss distribution for the simulated 3L-NPC converter at full power rating with a PF=1 for the silicon IGBT converter while Fig. 6.32 (b) shows the same plots for the SiC MOSFET converter. It can be seen from both Fig. 6.32 (a) and (b) that the outer transistors (T1 and T4 with respect to Fig. 6.27 (b)) are more electrothermally stressed and have the highest losses compared to the inner transistors (T2 and T3 with respect to Fig. 6.27 (b)).

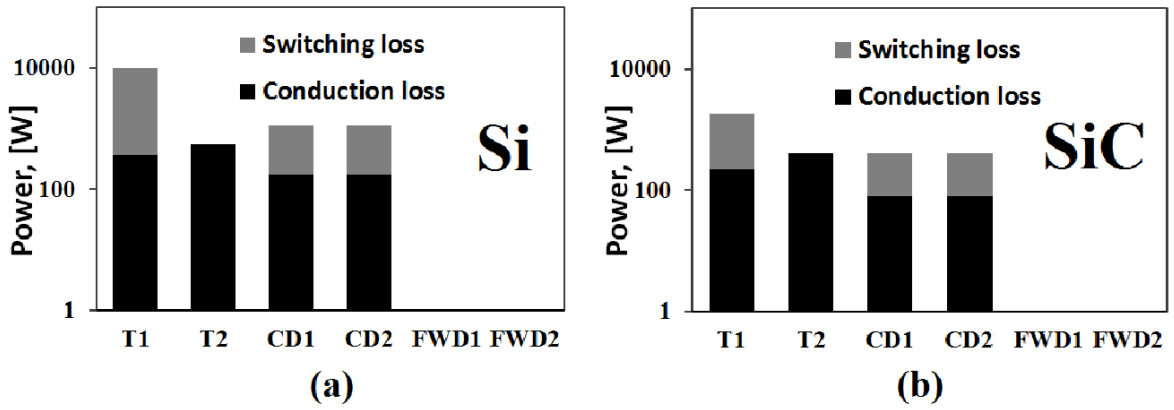


Fig. 6.32 Loss distribution in the 3L-NPC (PF=1): (a) Si; (b) SiC.

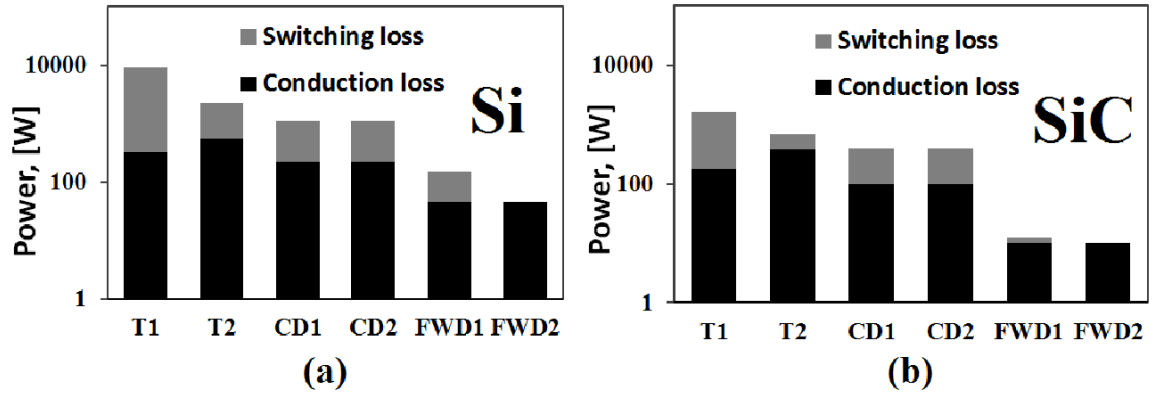


Fig. 6.33 Loss distribution in the 3L-NPC (PF=0.6): (a) Si; (b) SiC.

The losses in the SiC MOSFET converter are much lower and the FWDs are not stressed. Fig. 6.33 shows the loss distribution for Si and SiC case for a power factor equal to 0.6 where it can be seen that the losses in T2, the clamping diodes and the free-wheeling diodes increase with respect to Fig. 6.32. The higher losses in T1 and T4 for the case of PF=1 is due to the fact that when the large switching vectors are initiated, current is flowing through T1 or T4 as shown in Fig. 6.34 (a). As the power factor is reduced, the losses in the inner transistors (T2 and T3) increase while that of the outer transistors (T1 and T4) decrease. The thermal stress on the clamping and anti-parallel

diodes also increase at reduced power factors. This is because of the phase shift between the converter output voltage and the current i.e. when the large switching vectors are initiated, meaning T1 or T4 is ON, the current is not at its maximum, hence either T1 or T4 does not conduct current although it is ON as shown in Fig. 6.34 (b). Instead, FWDs start working more. For this power factor, the medium and small voltage vectors, where the inner transistors and clamping diodes are most used, conduct when the current is at its peak as shown in Fig. 6.34 (b).

Case temperature measurements have also been performed on each of the discrete devices in a phase leg of the single-phase 3L-NPC inverter shown in Fig. 6.27 (b). This was done by placing a thermal sensor on the case of each TO-247 device used in the converter as well as the clamping diodes connected to the neutral point. Measurements were done for 600 seconds for both the silicon IGBT and SiC MOSFET inverters and an SPWM switching technique was used. The DC link voltage was set to 500 V while the current was set at 700 mA. Since the current passed through the converter was very low, it was expected that the conduction losses would dominate over the switching losses. The switching frequency was 5 kHz.

Since the conduction losses on the inner transistors (T2 and T3) are greater than the conduction losses of the outer transistors (T1 and T4), then it is expected that the case temperatures of T2 and T3 will be higher under the conditions of the experimental measurements. The results of the temperature measurements are shown in Fig. 6.35 (a) for the silicon IGBT based converter and Fig. 6.35 (b) for the SiC based converter.

Indeed the case temperatures of the inner transistors are measured (T2 and T3) as higher than those of the outer transistors (T1 and T4).

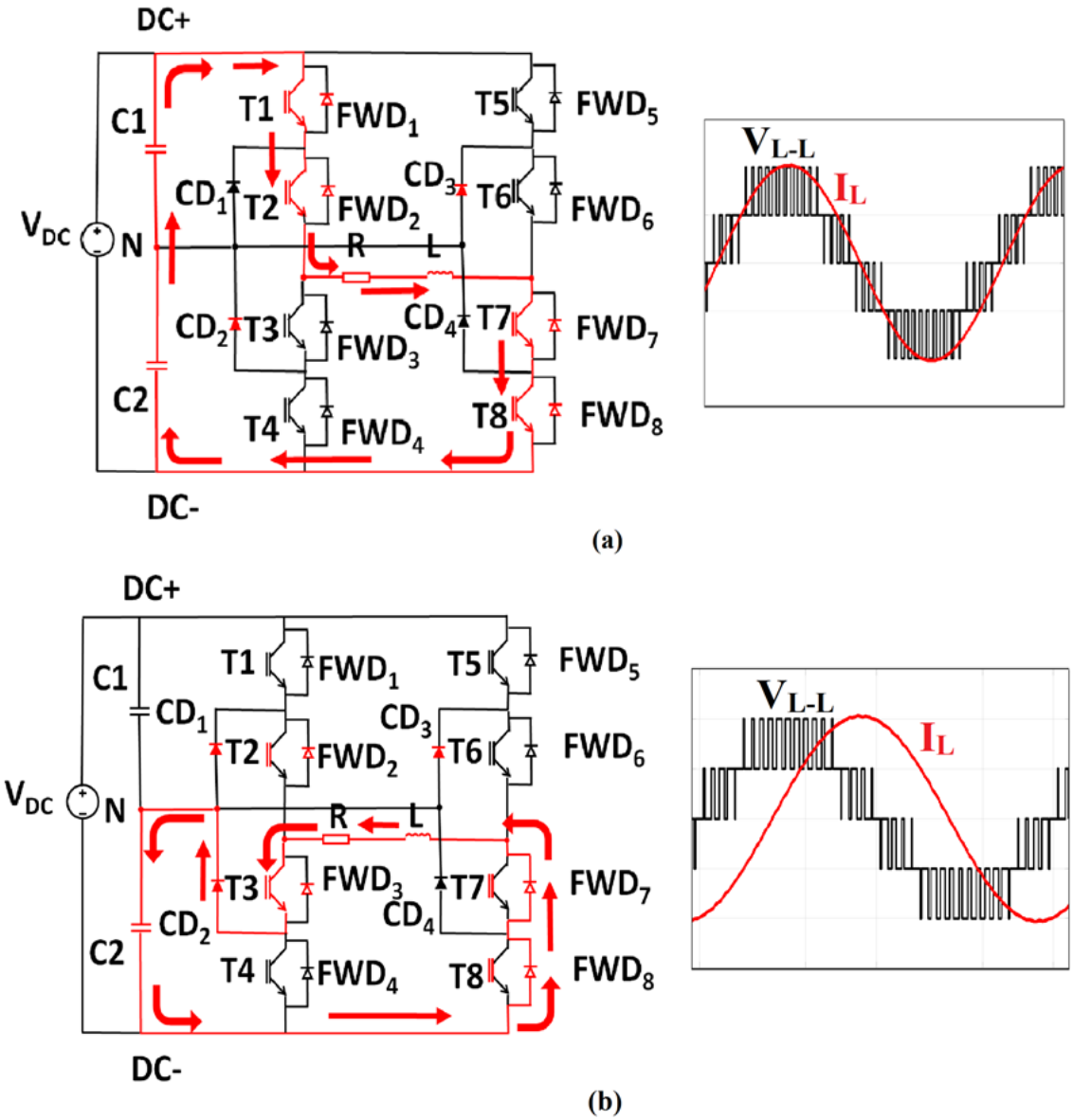


Fig. 6.34 Converter switching state and output voltage/current waveform for loads with a) PF=1 b) PF=0.6.

Under balanced conditions, where the upper and lower capacitor voltages are equal, the losses on the two inner transistors should be equal. Likewise, the losses on the two outer transistors should be equal. This is because the transistors have exactly the same switching pattern and duty ratio. This can be observed from the experimental measurements where the case temperatures of T1 and T4 are within 8.7% and the case temperatures of T2 and T3 are within 7.5%. Under unbalanced conditions, the transistor blocking the higher voltage will have higher switching losses and therefore exhibit a higher case temperature. This can be seen in the case temperature measurements shown in Fig. 6.36 (a) for the silicon IGBT 3L-NPC converter and Fig. 6.36 (b) for the SiC MOSFET 3L-NPC converter. In both cases, a high degree of capacitor voltage imbalance can be seen from the phase voltage measurements shown adjacent to the temperature plots. Here, the temperature difference between T1 and T4 increases from 8.7% in the balanced case to 48% in the unbalanced case. In the case of T2 and T3, the temperature difference under unbalanced conditions is 7.6%.

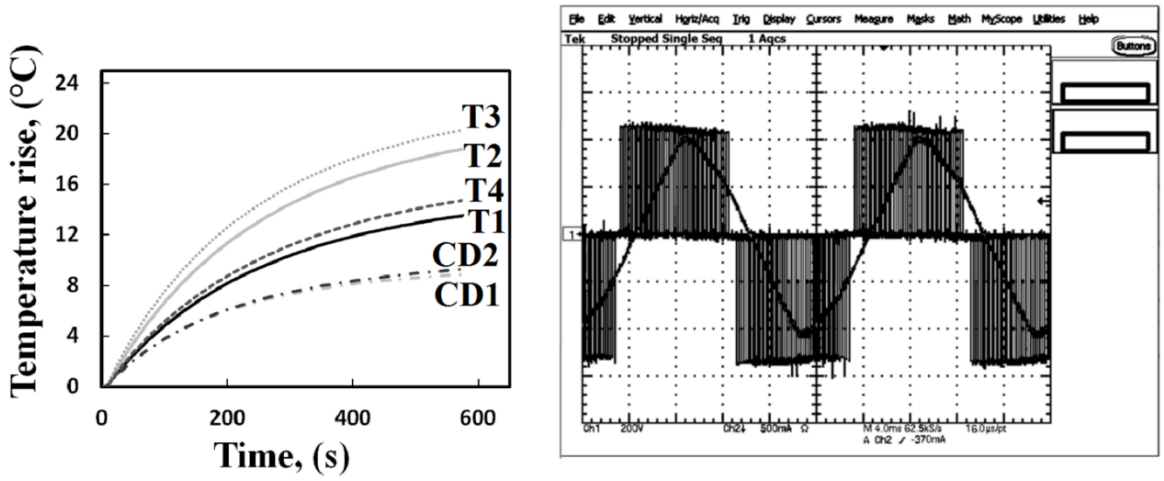
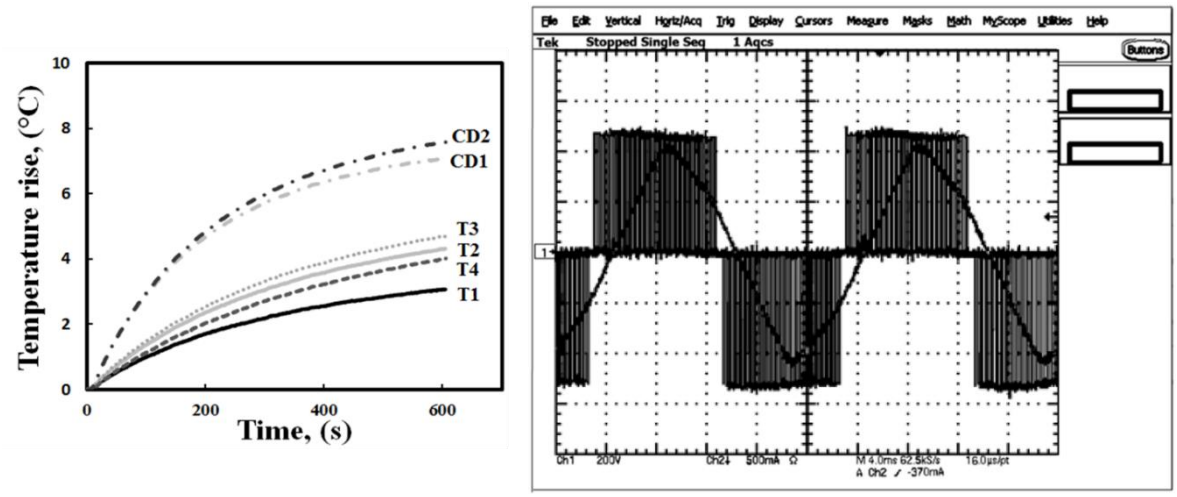


Fig. 6.35 (a). Temperature profile with balanced DC-link capacitors performance: T: Si IGBTs; CDs: PiN diodes



(b) T: SiC MOSFETs; CDs: Schottky diodes

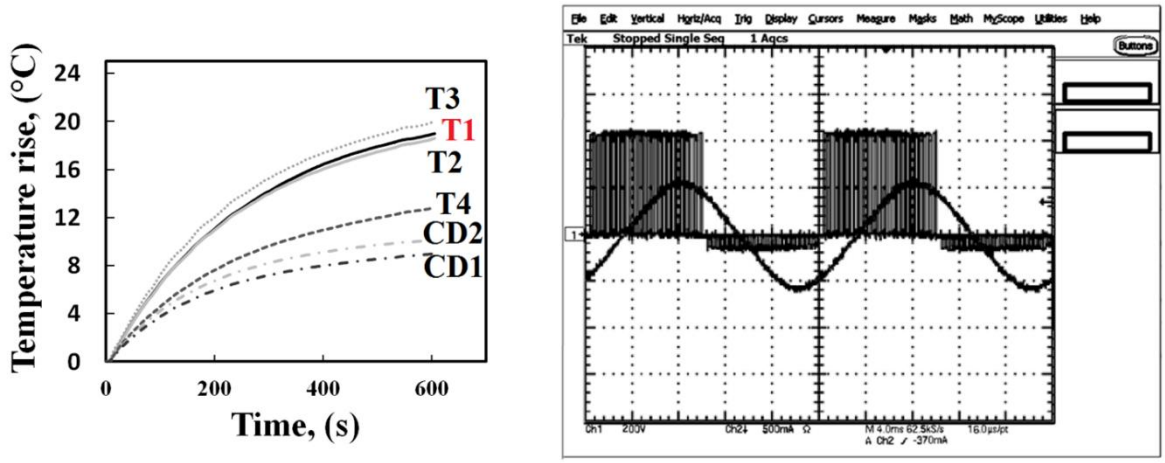
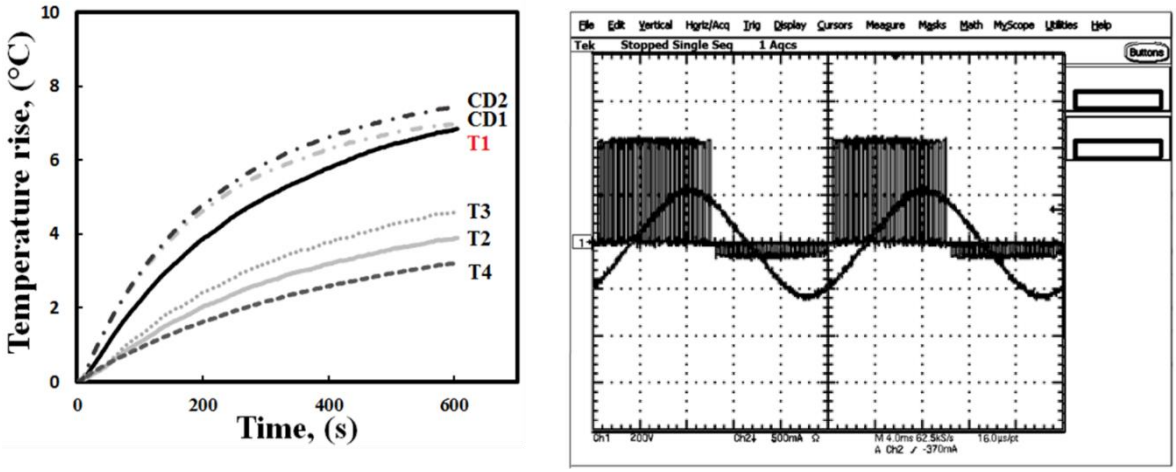


Fig. 6.36 Temperature profile with unbalanced DC-link capacitors performance: (a) T: Si IGBTs; CDs: PiN diodes



(b) T: SiC MOSFETs; CDs: Schottky diodes

6.5 Conclusion

In this chapter, a compact electrical drive model coupled with an electro-thermal power electronic model was developed in MATLAB/Simulink and used for driving a

permanent magnet synchronous motor through a 3L-NPC inverter. A motor control block based on field oriented control was developed which controlled the torque and incorporated a field weakening function in order to achieve the maximum torque at higher speed. An NEDC drive cycle was used to represent an actual drive scenario in which the motor was working in motoring, flux-weakening and regenerating modes. The model calculated the junction temperature of the device using a Cauer-thermal network and through a feedback loop, the losses of the inverter were updated after each time-step. In a drive application that uses a 3L-NPC inverter, the highly variable load makes the loss distribution less predictable. When the motor is operating in a drive cycle, as the motor accelerates and the speed increases the inverter is operating in the first quadrant and torque is positive. Here the outer transistors are more electrothermally stressed. In contrast, when the motor decelerates, it is working in the regenerative mode and torque is negative. Here, the inner transistors, clamping diodes and free-wheeling diodes become more stressed. Moreover, during the field weakening, when a reactive power is absorbed from the motor, the inner transistors become significantly more stressed. Hence, for 3L-NPC converters used in electric drive applications, a method of temperature profile prediction has been presented. This will be useful for reliability modelling.

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Chapter

7 Conclusion and Suggestions for Future Work

7.1 Conclusions

This thesis has used simulations in conjunction with experimental measurements to investigate the electrothermal performance of series connected power devices. The investigation of clamped inductive switching was performed on silicon and SiC power devices. In the analysis of voltage sharing of series connected devices during the static ON-state and OFF-state it was shown that the zero-temperature coefficient of the power devices determines the voltage sharing and loss distribution in the ON-state while the leakage current and switching synchronization is critical in the OFF-state.

In the investigations of the switching transient behaviour of series connected IGBT and SiC MOSFETs during Turn-OFF, this thesis has demonstrated the impact of different operating conditions (temperature and switching rate) on voltage sharing and compared the two technologies through experimental results justified by finite element models as well as compact Matlab/Simulink models. It was shown that the voltage imbalance for Si IGBT is highly dependent on the carrier concentration in the drift region during switching while for SiC MOSFET it depends on the switching time constant of the gate voltage and the rate that the MOS-channel cuts the current.

In snubberless circuits it is important to develop a technique for determining the Safe Operating Area for series connected devices, since the gate timing mismatch (loss of gate synchronization) can cause destructive failure from avalanche conduction. In the analysis of SOA of series connected devices it was discussed that the SOA is reduced by increased switching rates and DC link voltages. For a given switching rate, the maximum gate mismatch between the series devices to trigger avalanche induced failure reduces with increasing DC link voltage. Likewise, for a given DC link voltage, the maximum gate mismatch delay for triggering avalanche mode failure reduces with increasing switching rate. Hence, as far as maximizing the SOA is concerned, there is a trade-off between the DC link voltage and the switching rate.

In multilevel inverters, for example in 3-level NPC inverter, one device module might contain few series connected devices. Therefore it is important to know the electrothermal stresses within the inverter, since the in the 3L-NPC converter, depending on the application, the devices are not equally stressed, hence, the lifetime of the converter is dependent on the lifetime of the most stressed power device within it. Therefore, there is increasing focus on the thermal stresses and power loss distribution on the devices within the 3L-NPC converter. In a drive application that uses a 3L-NPC inverter, the highly variable load makes the loss distribution less predictable. When the motor is operating in a drive cycle, as the motor accelerates and the speed increases the inverter is operating in the first quadrant and torque is positive. Here the outer transistors are more electrothermally stressed. In contrast, when the motor decelerates, it is working in the regenerative mode and torque is negative. Here,

the inner transistors, clamping diodes and free-wheeling diodes become more stressed. Moreover, during the field weakening, when a reactive power is absorbed from the motor, the inner transistors become significantly more stressed.

7.2 Future Work

All the experiments of voltage sharing imbalance between series connected devices were limited to 2 series devices, so the next step is to use multiple devices more than two. This evaluation is more valuable for high voltage applications where multiple devices are used for high voltage applications for example, HVDC, FACTS or MMC applications.

It would be useful to test other WBG devices like GaN and to analyse the impact of these devices on voltage sharing of series connected devices. Current GaN based devices show advantages over Si and SiC devices in terms of switching speed, power losses and thermal features. However, these devices cannot be used in high voltage applications due to unavailability of them in high voltage ratings [1, 2]. Series connection of GaN devices can open a new field of study in increasing the voltage rating of these devices in high voltage applications.

Series connection of power devices is challenging due to the unbalanced voltage sharing between the devices, especially during the dynamic switching transients. There are few methods for balancing the voltage of the series connected devices such as: passive snubbers, active clamping circuits, gate signal delay method, and active gate control methods [3]. Passive devices (like *C*, *RC, RCD* etc.) can be used in parallel with the

switching device as passive snubbers. However, snubbers are bulky and exhibit higher switching losses that make them unattractive to use. In the active gate control method, the gate current is controlled by the gate drive to obtain the required outcome. Dynamic control of switching transient of power device during turn-on and turn-off is provided by the master-slaves control [4]. All those methods were considered and implemented for IGBTs. It is also important to analyse the behaviour of WBG devices using the active gate control methods as the switching dynamics as well as voltage sharing behaviour of these devices are different than the bipolar device behaviour.

7.3 References

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